Signetics

82S126
82S129
1K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 60ns max
- Input loading: -150μA max
- On-chip address decoding
- Two chip enable inputs
- Output options:
  - 82S126: Open collector
  - 82S129: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

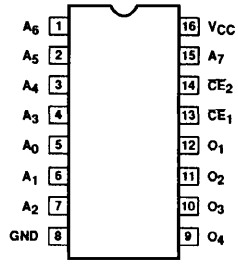
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	82S126/BEA, 82S129/BEA
16-pin Ceramic FlatPack	82S126/BFA, 82S129/BFA

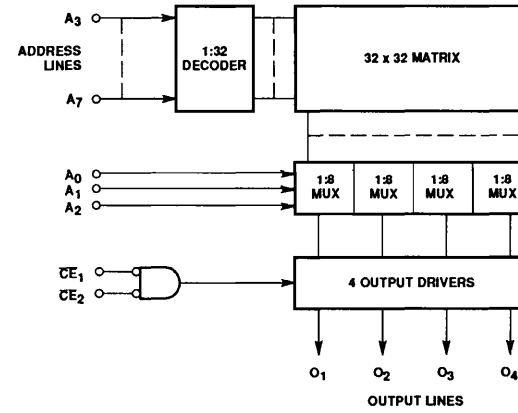
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S126)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S129)	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit TTL Bipolar PROM (256 × 4) — 82S126, 82S129

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High (82S129)	V_{CC} = 4.5V, I_O = -2.0mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 5.5V			40	µA
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 0.4V			-40	µA
I_{OS}	Short circuit (82S129)[3]	V_{CC} = 5.5V, $\overline{CE}_{1,2}$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{CC} = 5.5V			125	mA
Capacitance[6]						
		CE_1 or CE_2 = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		40	60	ns
t_{CE}	Access time[4]	Output	Chip Enable			30	ns
t_{CD}	Disable time	Output	Chip Disable			30	ns

NOTES:
1. *Positive current is defined as into the terminal referenced.*
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

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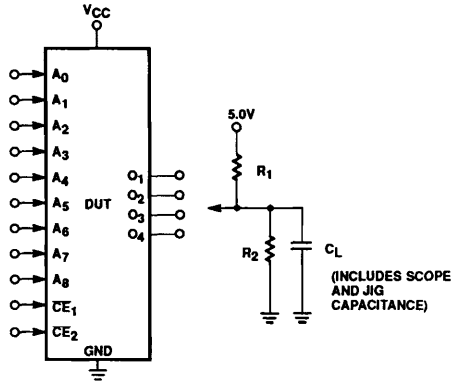
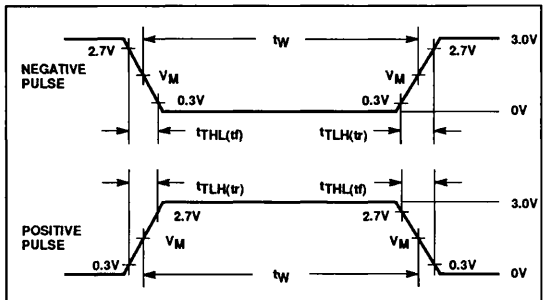
TEST LOAD CIRCUITS



NOTE:
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS