DESCRIPTION

The 82S146 and 82S147 are field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82S146 and 82S147 include on-chip decoding and one chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S146 and 82S147 devices are available in the commercial temperature range (0°C to +75°C), and are specified as N82S146/147, F.

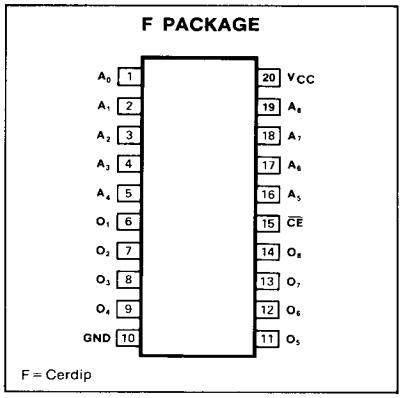
FEATURES

- **Address access time: 45ns max**
- **Power dissipation: 155mA max**
- **Input loading: -100μA max**
- **One chip enable input**
- **On chip address decoding**
- **Output options:**
  - **82S146: Open collector**
  - **82S147: Tri-state**
- **No separate fusing pins**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

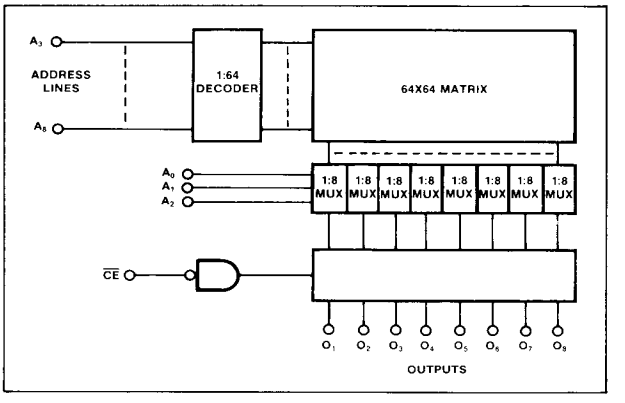
PIN CONFIGURATION



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	A_0	Address
2	A_1	Address
3	A_2	Address
4	A_3	Address
5	A_4	Address
6	O_1	Output
7	O_2	Output
8	O_3	Output
9	O_4	Output
10	GND	Ground
11	O_5	Output
12	O_6	Output
13	O_7	Output
14	O_8	Output
15	$\overline{CE}$	Chip enable bar
16	A_5	Address
17	A_6	Address
18	A_7	Address
19	A_8	Address
20	V_{CC}	Power supply voltage

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S146)	+5.5	
V_O	Off-state (82S147)	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$.

PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2	
	Output voltage					V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	
V_{OH}	High (82S147)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-100	
I_{IH}	High	V_{IN} = 5.5V			40	
	Output current					
I_{OLK}	Leakage (82S147)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
$I_{O(OFF)}$	Hi-Z state (82S147)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit (82S147)	V_{OUT} = 0V	-20		-70	mA
I_{CC}	V_{CC} supply current			115	155	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

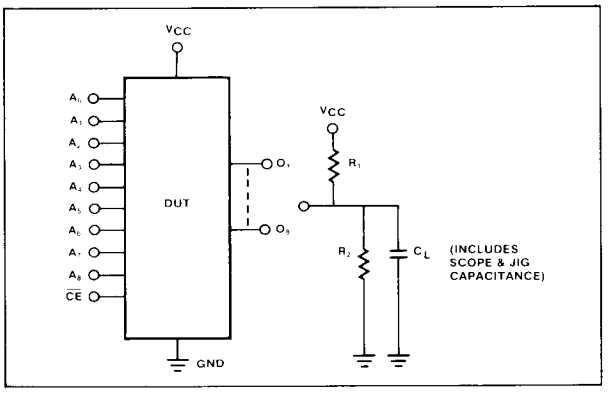
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, C_L = 30pF, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}		Output	Address		30	45	
T_{CE}		Output	Chip enable		20	30	
T_{CD}	Disable time	Output	Chip disable		20	30	ns

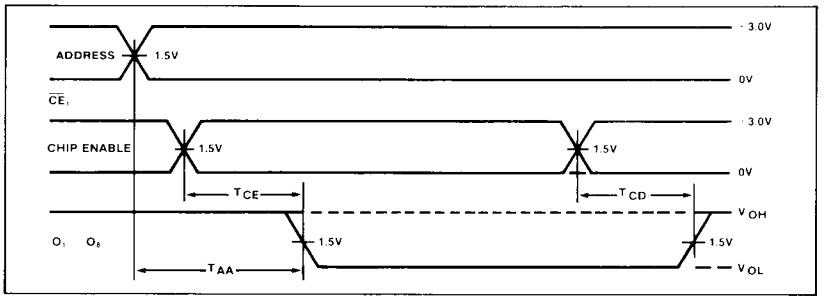
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] T_A = +25° C. (Testing of these limits may cause programming of device.)

PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			μs
t_P	$\overline{CE}$ programming pulse width		100		125	μs
t_D	Pulse sequence delay		5			μs
t_V	$\overline{CE}$ verify pulse width		1			μs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

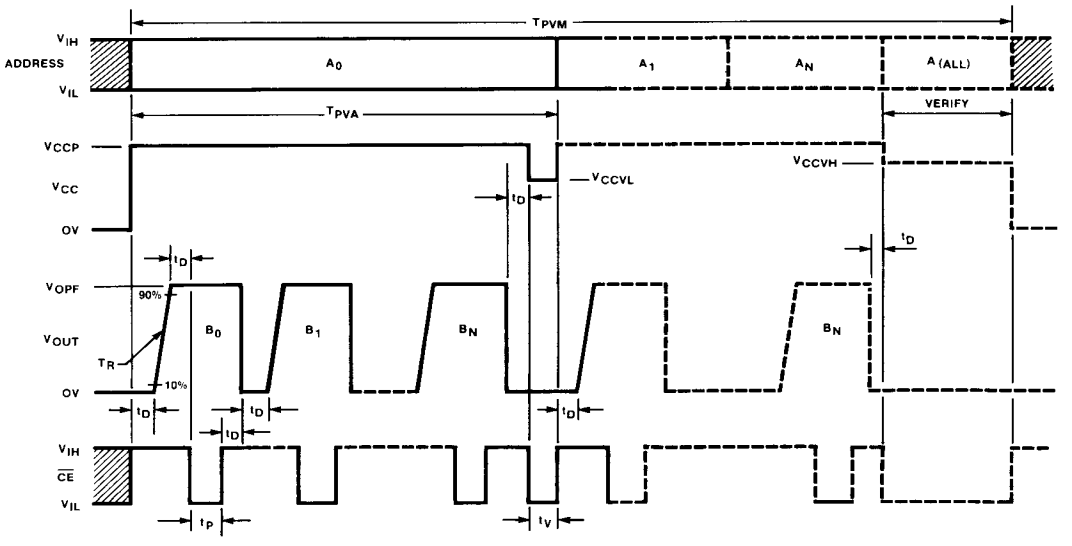
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}$ input to logic low for a time t_p.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.