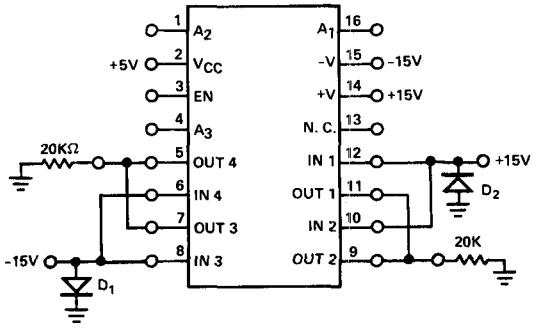
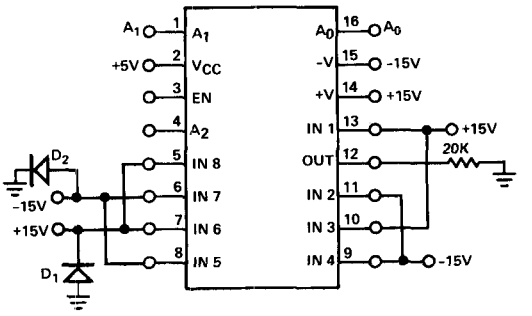
25 HI-1800A



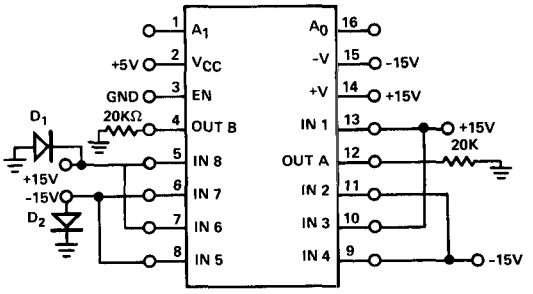
NOTES:
T_A = +125°C
A_1 = 100KHz
A_2 = 50KHz
A_3 = 25KHz
EN = 12.5KHz

26 HI-1818A



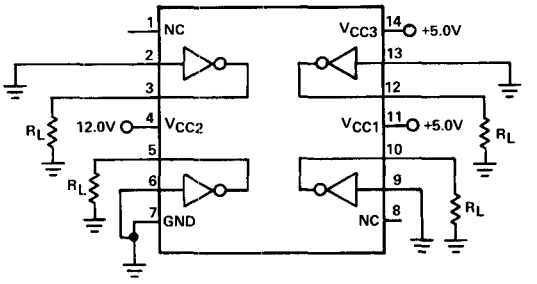
NOTES:
T_A = +125°C
A_0 = 100KHz
A_1 = 50KHz
A_2 = 25KHz
EN = 12.5KHz

27 HI-1828A



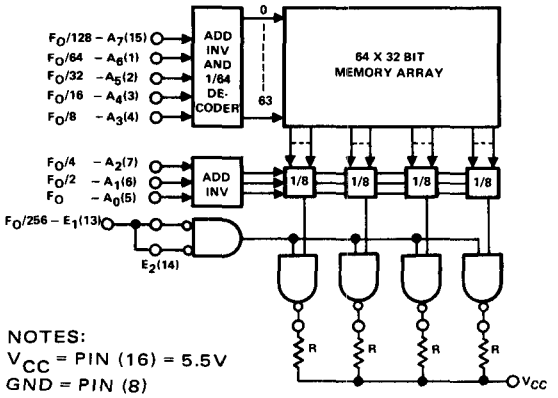
NOTES:
T_A = +125°C
A_0 = 100KHz
A_1 = 50KHz
EN = 25KHz

28 HD-6600/6605



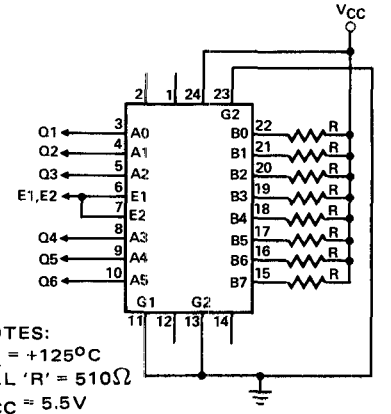
NOTES:
T_A = +125°C
R_L = 39Ω
All V_{CC} = ± 10%

29 HM-7610/7611



NOTES:
V_{CC} = PIN (16) = 5.5V
GND = PIN (8)
R = 300Ω
F_O = 100KHz Square Wave
T_A = +125°C

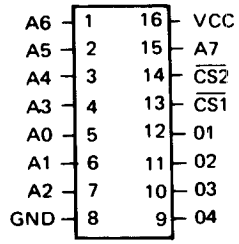
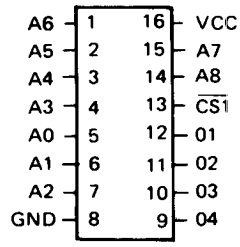
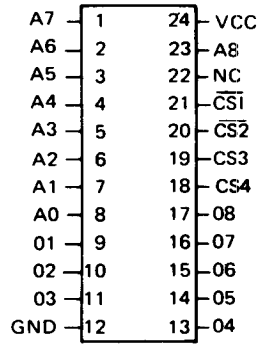
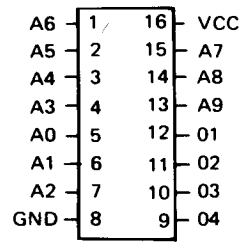
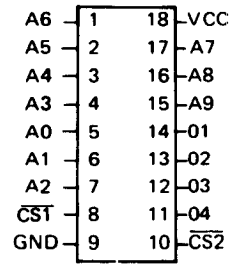
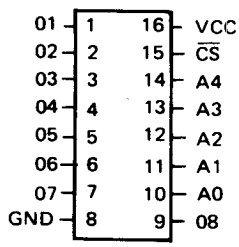
30 HPROM-0512



NOTES:
T_A = +125°C
ALL 'R' = 510Ω
V_{CC} = 5.5V
FREQ:
Q_1 = 100KHz, Q_2 = 50KHz
Q_3 = 25KHz, Q_4 = 12.5KHz
Q_5 = 6.15KHz, Q_6 = 3.12KHz
E1 = E2 = 1.5625KHz

DASH 8

HARRIS GENERIC PROM PRODUCT CHART

ORGANIZATION	PART NUMBER	OUTPUT TYPE	PINOUT	MAXIMUM ACCESS OVER VOLTAGE AND TEMP.	TYPICAL PROGRAMMING TIME (ALL BITS)
256 X 4	HM-7610 HM-7611	(OC) (TS)		60ns	1 SECOND
512 X 4	HM-7620 HM-7621	(OC) (TS)		70ns	2 SECONDS
512 X 8	HM-7640 HM-7641	(OC) (TS)		70ns	4 SECONDS
1024 X 4	HM-7644	ACTIVE PULLUP		70ns	4 SECONDS
1024 X 4	HM-7642 HM-7643	(OC) (TS)		70ns	4 SECONDS
32 X 8	HM-7602 HM-7603	(OC) (TS)		40nsec	<1 SECOND

MEMORY

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HM-7610/7611

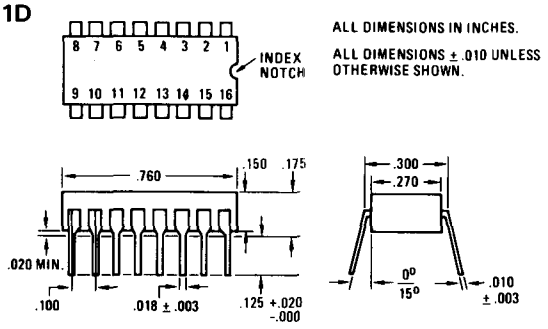
1024-Bit Field Programmable Bipolar PROM

FEATURES

- 256 Words, 4-Bits per Word
- Simple, High Speed Programming Procedure (less Than 1 Second Typical)
- Inputs and Outputs TTL Compatible
  - ▶Low Input Current -400 μA Logic "0", 40 μA Logic "1"
  - ▶Full Output Drive -15mA Sink/2mA Source
- Fast Access Time–60NS Over Commercial Temperature & Voltage, 75NS Over Military Temperature & Voltage
- Expandable – "Wired-Or" Outputs With Chip Select
- Pin Compatible With Industry Standard 256 X 4 Proms

PACKAGE

CODE 1D



DESCRIPTION

The HM-7610 (open collector) and HM-7611 (three-state) are fully decoded, high speed, 1024-bit programmable ROM'S organized as 256 words by 4 bits per word. They are supplied with all bits storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low).

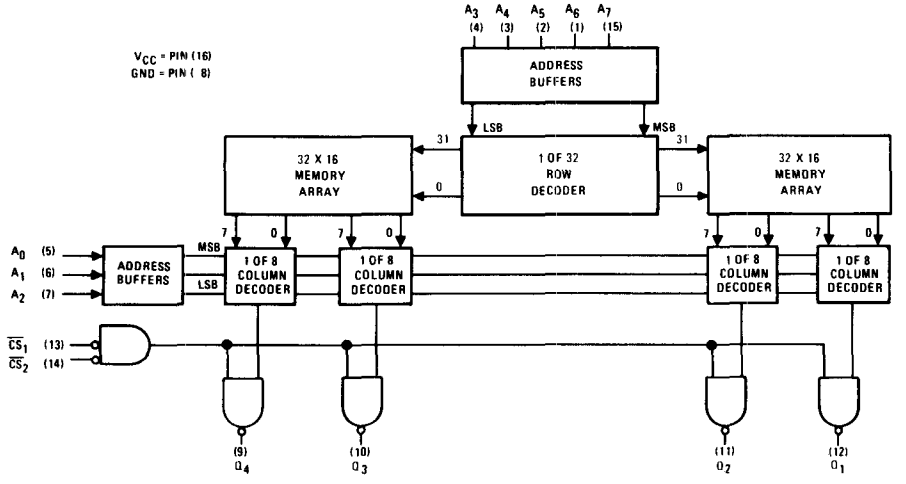
The nichrome fuse technology is the same as is used in the JAN approved MIL 38510/201 PROM, and in all other Harris PROMS.

The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides extremely fast access time, and features temperature and voltage compensation to minimize variations in access time.

The pinout is compatible with the industry standard 256X4 PROM.

In addition to the conventional storage array, two test rows and two test columns are included to assure high programmability, and guarantee parametric and A.C. performance. Fuses in these test rows and columns are blown prior to shipment.

BLOCK DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	7.0V
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+150°C
Operating Temperature (Ambient)	+125°C
Maximum Junction Temperature	+175°C

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (OPERATING)

				HM-7610-5			HM-7611-5				
			V_{CC}	5V ±5%			5V ±5%				
			TA	0°C to +70°C			0°C to +70°C				
	PARAMETER		SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
D.C.	Address/Enable Input Current	"1"	I_{RA}, I_{RE}		0	40		0	40	µA	$V_{IH} = V_{CC}$ Max
		"0"	I_{FA}, I_{FE}		-0.1	-0.4		-0.1	-0.4	mA	V_{IL} = 0.45V
	Input Threshold Voltage	"1"	V_{IH}	2.0			2.0			V	$V_{CC} = V_{CC}$Min
		"0"	V_{IL}			0.8			0.8	V	$V_{CC} = V_{CC}$Max
	Output Voltage	"1"	V_{OH}	N/A			2.4	3.4		V	I_{OH} =-2.0mA, $V_{CC} = V_{CC}$Min
		"0"	V_{OL}		0.35	0.45		0.35	0.45	V	I_{OL} = +15mA, $V_{CC} = V_{CC}$Min
											$V_{CS_1} = V_{CS_2}$ = 0.8V
	Output Disabled Current	"1"	$I_{OH\overline{E}}$			100			100	µA	$V_{OH}, V_{CC} = V_{CC}$ max
		"0"	$I_{OL\overline{E}}$			N/A			-100	µA	V_{OL} = +0.3V, $V_{CC} = V_{CC}$ Max
											$V_{CS_1} = V_{CS_2}$ = 2.0V
	Output Leakage	"1"	I_{OH}			100			N/A	µA	$V_{OH}, V_{CC} = V_{CC}$ Max
	Power Supply Current		I_{CC}		90	130		90	130	mA	$V_{CC} = V_{CC}$ Max All Inputs Grounded
	Input Clamp Voltage		V_{CL}			-1.5			-1.5	V	I_{in} = -10ma
	Output Short Circuit Current		I_{OS}	N/A		N/A	15	23	30	mA	$V_{CC} = V_{CC}$ Max, V_{OUT} = 0.0V One output only for a Max of 1 sec
A.C.	Address Acces Time		t_{AA}		40	60		40	60	ns	V_{CC} and T_A Over Full Range
	Enable Access Time		t_{EA}		15	25		15	25	ns	V_{CC} and T_A Over Full Range

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

				HM-7610-2			HM-7611-2				
			V_{CC}	5V ±10%			5V ±10%				
			TA	-55°C to +125°C			-55°C to +125°C				
	PARAMETER		SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
D.C.	Address/Enable Input Current	"1"	I_{RA}, I_{RE}		0	40		0	40	µA	$V_{IH} = V_{CC}$ Max
		"0"	I_{FA}, I_{FE}		-0.1	-0.4		-0.1	-0.4	mA	V_{IL} = 0.45V
	Input Threshold Voltage	"1"	V_{IH}	2.0			2.0			V	$V_{CC} = V_{CC}$ Min
		"0"	V_{IL}			0.8			0.8	V	$V_{CC} = V_{CC}$ Max
	Output Voltage	"1"	V_{OH}	N/A			2.4	3.4		V	I_{OH} = -2.0mA; $V_{CC} = V_{CC}$ Min
		"0"	V_{OL}		0.35	0.45		0.35	0.45	V	I_{OL} = +15mA; $V_{CC} = V_{CC}$ Min
											$V_{CS_1} = V_{CS_2}$ = 0.8V
	Output Disabled Current	"1"	$I_{OH\overline{E}}$			100			100	µA	$V_{OH}, V_{CC} = V_{CC}$ Max
		"0"	$I_{OL\overline{E}}$			N/A			-100	µA	V_{OL} = +0.3V, $V_{CC} = V_{CC}$ Max
											$V_{CS_1} = V_{CS_2}$ = 2.0V
	Output Leakage	"1"	I_{OH}			100			N/A	µA	$V_{OH}, V_{CC} = V_{CC}$ Max
	Power Supply Current		I_{CC}		90	130		90	130	mA	$V_{CC} = V_{CC}$ Max All Inputs Grounded
	Input Clamp Voltage		V_{CL}			-1.5			-1.5	V	I_{in} = -10ma
	Output Short Circuit Current		I_{OS}	N/A		N/A	15	23	30	mA	$V_{CC} = V_{CC}$ Max, V_{OUT} = 0.0V One output only for a Max of 1 sec
A.C.	Address Access Time		t_{AA}		40	75		40	75	ns	V_{CC} and T_A Over Full Range
	Enable Access Time		t_{EA}		15	30		15	30	ns	V_{CC} and T_A Over Full Range

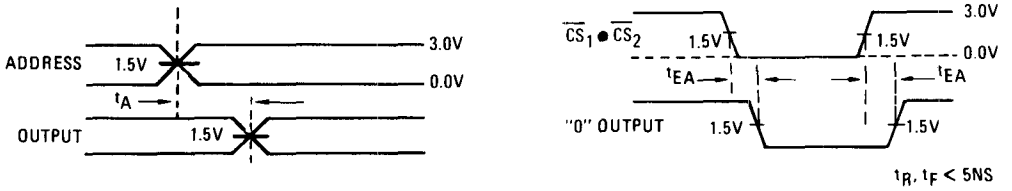
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

CAPACITANCE (1): T_A = 25°C

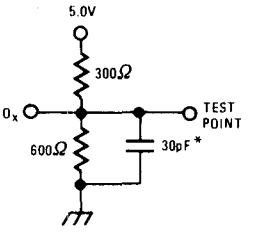
PARAMETER	SYMBOL	TYP.	UNITS	TEST CONDITION
Add. Input Cap.	$C_{IN\ A, CS}$	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
Output Cap.	C_{OUT}	8	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

NOTE: (1) These parameters are only periodically sampled and are not 100% tested.

SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



*Includes jig & probe total capacitance

PROGRAMMING

The HM-7610/7611 is manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. The HM-7610/7611 can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

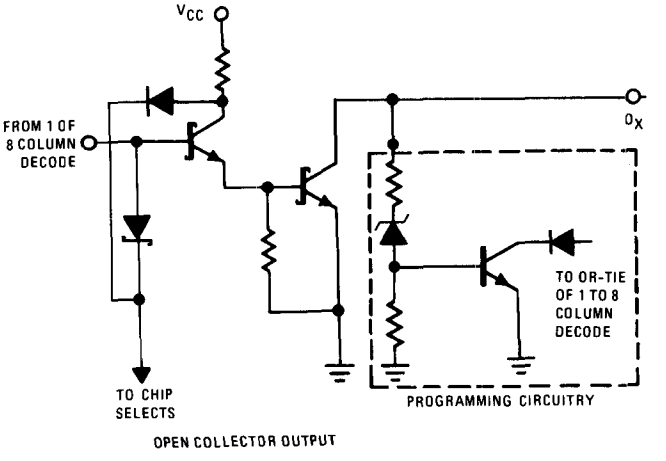
TABLE 1

PARAMETER	SYMBOL	MIN.	RECOMMEND VALUE	MAX.	UNITS
Address Input Voltage (1)	V_{IH} V_{IL}	2.4 0.0	5.0 0.4	5.0 0.8	V V
Programming/Verify Voltage to V_{CC} (2)	V_{PH} V_{PL}	11.5 3.75	12.0 4.0	12.5 4.25	V
Programming Voltage Current Limit	I_{CCP}			600	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r t_f	1 1	1 1	10 10	μs μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width – First Attempts	t_{p1}	100	100	200	μs
Programming Pulse Width – Subsequent	t_{p2}	10	10	20	ms
Programming Duty Cycle	D.C.	–	10	10	%
Output Voltage Enable Disable (3)	V_{OPE} V_{OPD}	9.5 0	10.0 .45	10.5 5.5	V V
Output Voltage Enable Current Limit	I_{OPE}			10	mA
Case Temp	T_C			75	°C

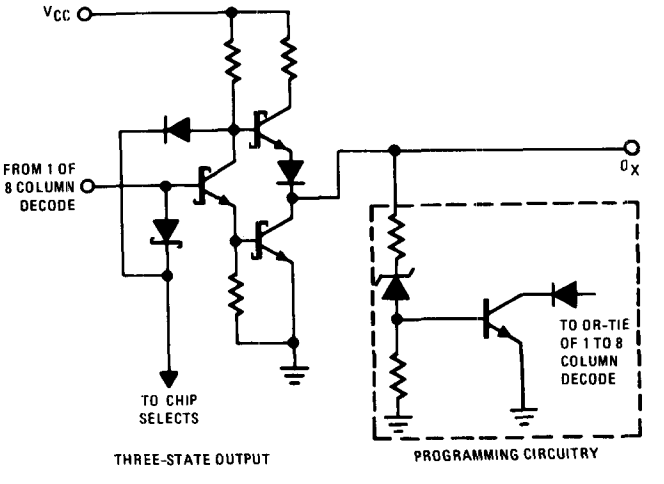
1. Address and chip select should not be left open for V_{IH}.
2. Verification at V_{CC} = 4.0 ± .25 Volts, T_A = 25°C is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

SCHEMATIC DIAGRAMS

HM-7610



HM-7611



MEMORY

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to both chip select inputs. The chip select inputs are TTL compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open circuit to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude equal to V_{OPE} and duration of t_{p1} to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.0 ± .25 Volts following a delay to t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}_1$ and $\overline{CS}_2$ inputs.
9. If any bit does not verify as programmed, repeat steps 2 through 8 using an output pulse enable width of t_{p1} for up to 15 additional pulses to enhance programming speed. If the bit is still unprogrammed, follow with at least 16 repetitive pulses of t_{p2} in width, to achieve high programming yield. In the event that the bit is still unprogrammed, the part is considered a programming reject and should be returned to the factory. The address and incorrect and desired contents of a location in which a programming failure has occured in any returned device must be included with that return.
10. Repeat steps 1 thru 9 for all other bits to be programmed in the PROM.

RECOMMENDED PROGRAMMING CIRCUIT

The circuit and timing diagram shown in Figures 1 and 2 will establish the proper programming condition for the output enable pulse. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand input up to 12.5 Volts during programming.

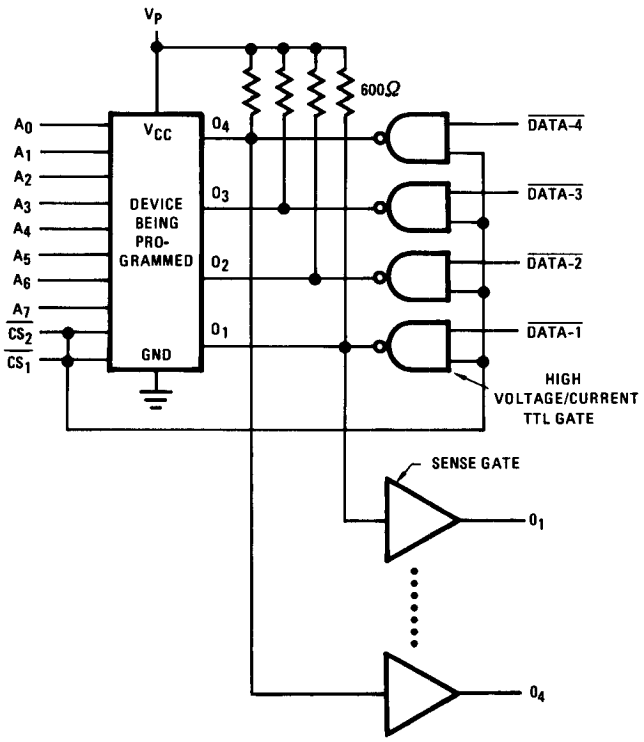


FIGURE 1

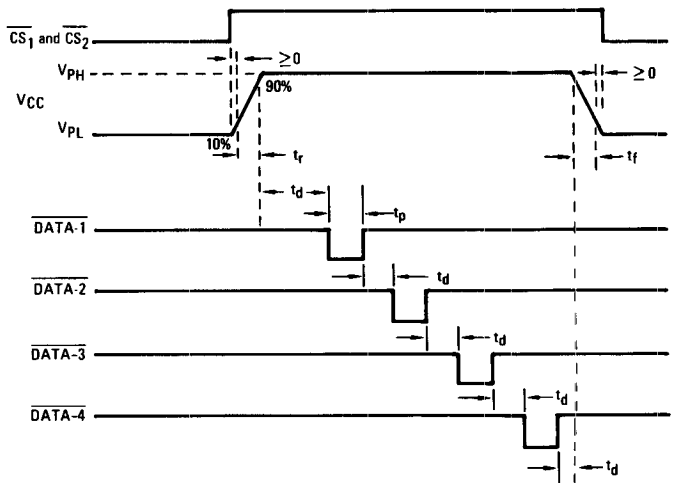


FIGURE 2