FUJITSU
CMOS 1M-BIT MASK-PROGRAMMABLE READ ONLY MEMORY
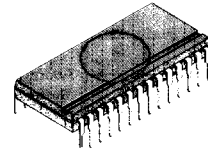
MB831000-15
MB831000-20

1M-BIT (131,072 x 8) CMOS READ ONLY MEMORY

The Fujitsu MB 831000 is a CMOS Si-gate mask-programmable static read only memory organized as 131,072 words by 8 bits.
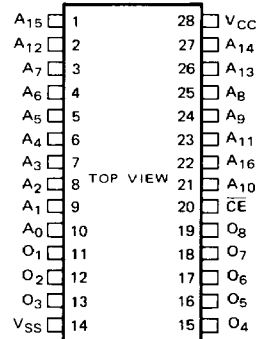
The MB 831000 has TTL-compatible I/O and 3-state output level with fully-static operation (i.e. no need of clock signal) and a single +5V power supply is required. Also, the MB 831000 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

- Organization: 131,072 words x 8 bits
- Access time: 150 ns (MB 831000-15)
  200 ns (MB 831000-20)
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5V power supply
- Power dissipation: 220 mW max. (Active)
  16.5 mW max. (Standby, TTL input level)
  275 μW max. (Standby, CMOS input level)
- Standard 28-pin DIP

PLASTIC PACKAGE
DIP-28P-M02

PIN ASSIGNMENT

A_{15}	1	28	V_{CC}
A_{12}	2	27	A_{14}
A_7	3	26	A_{13}
A_6	4	25	A_8
A_5	5	24	A_9
A_4	6	23	A_{11}
A_3	7	22	A_{16}
A_2	8	21	A_{10}
A_1	9	20	$\overline{CE}$
A_0	10	19	O_8
O_1	11	18	O_7
O_2	12	17	O_6
O_3	13	16	O_5
V_{SS}	14	15	O_4

TOP VIEW

ABSOLUTE MAXIMUM RATINGS (See NOTE)

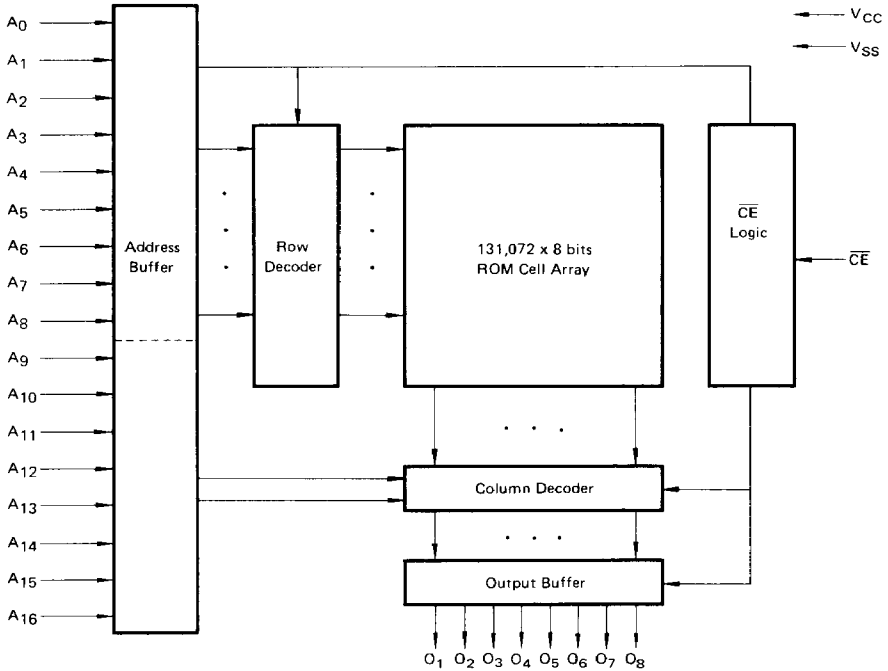| Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0*	V
Input Voltage	V_{IN}	−0.5 to V_{CC}+0.5*	V
Output Voltage	V_{OUT}	−0.5 to V_{CC}+0.5*	V
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

* Referenced to GND

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 — MB 831000 BLOCK DIAGRAM

Inputs A_0–A_{16} → Address Buffer → Row Decoder → 131,072 x 8 bits ROM Cell Array

CE Logic → $\overline{CE}$

V_{CC}, V_{SS}

Column Decoder

Output Buffer

Outputs O_1 O_2 O_3 O_4 O_5 O_6 O_7 O_8

TRUTH TABLE

$\overline{CE}$	MODE	Output	Power Dissipation Mode
H	Not selected	High-Z	Standby
L	Selected	Output	Active

CAPACITANCE ($T_A = 25°C$, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance ($V_{OUT} = 0V$)	C_{OUT}			10	pF
Input Capacitance ($V_{IN} = 0V$)	C_{IN}			7	pF

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

| Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Condition
Active Supply Current	I_{CC}		40	mA	$\overline{CE} = V_{IL}$, Minimum Cycle
Standby Supply Current	I_{SB1}		3	mA	$\overline{CE} = V_{IH}$
	I_{SB2}		50	μA	$\overline{CE} = V_{CC}$, V_{IN} = GND or V_{CC}
Input Leakage Current	I_{LI}	−10	10	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−10	10	μA	$\overline{CE} = V_{IH}$
Output High Voltage	V_{OH}	2.4		V	$I_{OH} = -400\mu A$
Output Low Voltage	V_{OL}		0.4	V	$I_{OL} = 2.1mA$

Fig. 2 — AC TEST CONDITION

Input Pulse Level   : 0.6 to 2.4 V
Input Pulse Rise and Fall Time : t_T = 10 ns
Timing Reference Levels   : Input: V_{IL} = 0.8 V, V_{IH} = 2.2V
                           : Output: V_{OL} = 0.8 V, V_{OH} = 2.2V
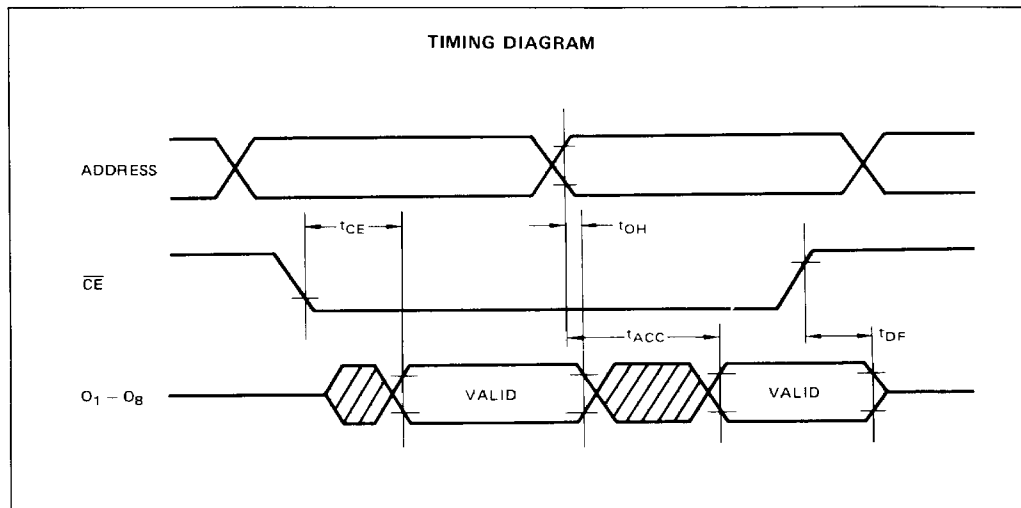Output Load   : 1 TTL Gate and 100pF
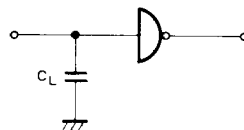
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB 831000-15		MB 831000-20		Unit
		Min	Max	Min	Max	
Address Access Time	t_{ACC}		150		200	ns
Chip Enable Access Time	t_{CE}		150		200	ns
Output Disable Time	t_{DF}		60		60	ns
Output Hold Time	t_{OH}	0		0		ns

TIMING DIAGRAM

MB 831000 ROM CODE DATA INPUT METHOD

Fujitsu's preferred method of receiving ROM Code Data is in the form of Programmed EPROMs or Magnetic Tapes.
Fujitsu produces the Masks in accordance with the Data in received EPROMs or Magnetic Tapes using Fujitsu computer systems.

MASK ROM CODE DATA RELEASE BY EPROMS:

● 128K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use 8 pcs of MBM 27128 or equivalent and program data of 8 address blocks (Address 0 to 16 K, 16 K to 32 K, 32 K to 48 K, 48 K to 64 K, 64 K to 80 K, 80 K to 96 K, 96 K to 112 K and 112 K to 128 K) of MB 831000 to each MBM 27128 EPROM. Fujitsu requires 3 sets, total 24 pcs, of such programmed EPROMs. (Two sets, total 16 pcs, are acceptable.)
In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (8 pcs) for supplying customer ROM Data Code verification.

MSB   LSB

A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	MBM 27128 (No. 1: 0 to 16 K)													
0	0	1	MBM 27128 (No. 2: 16 K to 32 K)													
0	1	0	MBM 27128 (No. 3: 32 K to 48 K)													
0	1	1	MBM 27128 (No. 4: 48 K to 64 K)													
1	0	0	MBM 27128 (No. 5: 64 K to 80 K)													
1	0	1	MBM 27128 (No. 6: 80 K to 96 K)													
1	1	0	MBM 27128 (No. 7: 96 K to 112 K)													
1	1	1	MBM 27128 (No. 8: 112 K to 128 K)													

● 256K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use 4 pcs of MBM 27C256 or equivalent and program data of 4 address blocks (Address 0 to 32K, 32K to 64K, 64K to 96K and 96K to 128K) of MB 831000 to each MBM 27C256 EPROM.
Fujitsu requires 3 sets, total 12 pcs, of such programmed EPROMs. (Two sets, total 8 pcs, are acceptable.)
In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (4 pcs) for supplying customer ROM Data Code verification.

MSB   LSB

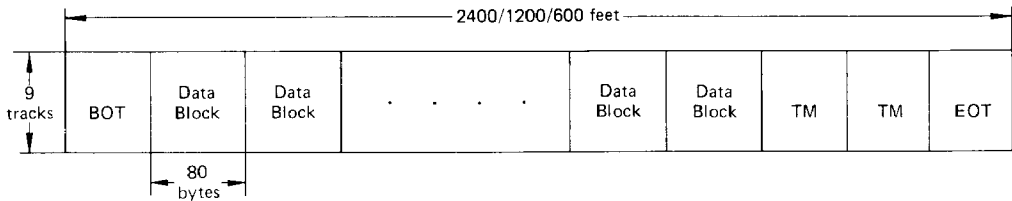| A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	MBM 27C256 (No. 1: 0 to 32 K)														
0	1	MBM 27C256 (No. 2: 32 K to 64 K)														
1	0	MBM 27C256 (No. 3: 64 K to 96 K)														
1	1	MBM 27C256 (No. 4: 96 K to 128 K)														

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MASK ROM CODE DATA RELEASE BY MAGNETIC TAPES:

When the customer releases his Mask ROM Code Data in the form of Magnetic Tapes (MT), he should use tapes that can be used on IBM compatible equipment and meet the following requirements.

● Physical Requirements:

1 Length : 2400 feet, 1200 feet, or 600 feet
2 Width : 1/2 inch
3 Track : 9 tracks
4 Density : 800 BPI or 1600 BPI

● MT Format:

1 Label : No tape mark on the header of tape
2 Record Size : 80 bytes/record
3 Block Size : Single record/block
4 File : Single file/volume
5 Code Used : EBCDIC code

```
         |◄───────────────────── 2400/1200/600 feet ─────────────────────►|
  9     |     | Data  | Data  |             | Data  | Data  |      |      |      |
tracks  | BOT | Block | Block |  .  .  .  . | Block | Block |  TM  |  TM  | EOT  |
         |     |◄─ 80 ─►|
              bytes
```

Note: BOT : Beginning of Tape
      EOT : End of Tape
      TM : Tape mark

Data Block Format:

Row Number	1 9	10 15	16 19	20 67	68 72	73 80
	Undefined Field	Address Field (1 Head Address)	Undefined Field	Data Field (16 words)	Undefined Field	Sequence
Number of Byte	9 bytes	6 bytes	4 bytes	48 bytes	5 bytes	8 bytes

Note: 1 byte/row

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Undefined Filed (Row 1~9/Row 16~19/Row 68~72):

In this field, blanks (b̄) should be recorded.

Address Field (Row 10~15):

In the address field, the header address of the 16-word data that follow the address field should be recorded in the form of a five-digit hexadecimal number following a symbol "#". The correspondence of actual binary address to this hex address is shown in the following example.

MSB																LSB
Address Bit	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Binary Address	0	0	0	1	1	1	0	1	1	1	0	0	1	0	0	1	0
Hex Address	0		3			B			9			2					
Recorded Form	#03B92																

Data Field (Row 20 ~ 67):

In this field, 16-word data with 16 successive addresses should be recorded in the form of two-digit hexadecimal numbers followed by a blank (b̄). (The header data is for the address recorded in the address field.) The correspondence of actual binary data to this hex data is shown in the following example.

Data Bit	08	07	06	05	04	03	02	01
Binary Data	1	1	1	1	0	0	1	0
Hex Data	F				2			
Recorded Data	F2b̄							

Sequence Number field (Row 73 ~ 80)

In this field, the sequence number of each record (data block) should be recorded in the form of an eight-digit decimal number, which must be counted up by tens. All digits to the left of the most significant digit should be zeros, not blanks. Refer to the following example.

Address		Data						Sequence No.	
10	15	20	22	23	25	65	67	73	80
#03B92		F2b̄		A0b̄		· · · ·	07b̄	00000010	

PACKAGE DIMENSIONS

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28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)

(EJECTOR MARK)

INDEX

15°MAX

.543±.010
(13.8±0.25)

.600(15.24)TYP

$1.407^{+.008}_{-.012}(35.73^{+0.2}_{-0.3})$

.010±.002
(0.25±0.05)

.062(1.58)MAX

$.039^{+.020}_{-0}$ $(0.99^{+0.5}_{-0})$

.195(4.96)MAX

.118(3.0)MIN

.100(2.54)
TYP

$.060^{+.020}_{-0}$
$(1.52^{+0.5}_{-0})$

.018±.003
(0.46±0.08)

.020(0.51)MIN

Dimensions in
inches (millimeters)

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