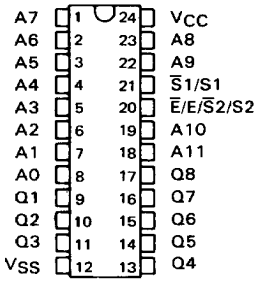
MAY 1977 – REVISED NOVEMBER 1985

- 4096 X 8 Organization
- All Inputs and Outputs TTL Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time from Address
  TMS4732-15 150 ns
  TMS4732-20 200 ns
  TMS4732-25 250 ns
- Pin-Compatible with TMS2532 EPROM
- Optional Power Down or Chip Select
- Two Output-Enable Controls for Chip Select Flexibility
- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 82.5 mW

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
Ē/E/S̄2/S2	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
S̄1/S1	Chip Select
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS4732 is a 32,768-bit read-only memory organized as 4,096 words of 8-bit length. This makes the TMS4732 ideal for microprocessor-based systems. The device is fabricated using N-channel self-aligned silicon-gate technology for high speed and simple interface with bipolar and CMOS circuits.

The TMS4732 is fully compatible with Series 74, 74S, or 74LS TTL and CMOS logic. The data outputs are three state for OR-tying multiple devices on a common bus. Pins 20 and 21 are mask programmable, providing additional system flexibility. The data at the outputs is always available during a read cycle. It is not dependent on external clocking of pins 20 and 21.

This ROM is supplied in a 24-pin dual-in-line plastic (N suffix) package designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address.

chip selects (S̄1 or S1 and S̄2 or S2)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a low-level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

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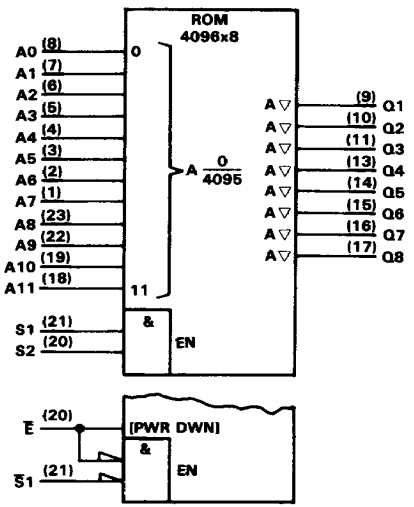
chip enable/power down ($\overline{E}$ or E) or chip select ($\overline{S}2$ or S2)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S}2$ or S2). Each option can be active high or active low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 15 mA. With pin 20 programmed as a chip-select pin, it is functionally identical to pin 21.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20 and 21 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pins 20 and 21 can be active high as shown in the upper symbol or active low as shown in the lower (partial) symbol. In addition, pin 20 can be either a second chip-select ($\overline{S}2$ or S2) or a chip-enable/power-down ($\overline{E}$ or E) pin.

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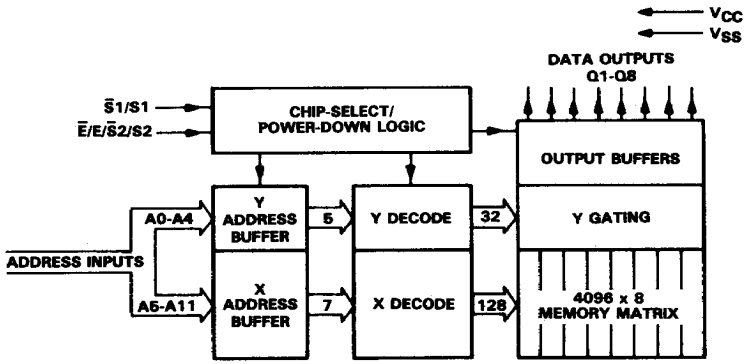
functional block diagram



absolute maximum ratings

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range (see Note 1) . . . . . −1 V to 7 V
Input voltage range (see Note 1) . . . . . −1 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = -1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0 V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			15	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ± 10% (see Figure 1)†

PARAMETER		TMS4732-15		TMS4732-20		TMS4732-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250	ns
$t_{a(S)}$	Access time from chip select		120		120		120	ns
$t_{a(PD)}$	Access time from chip enable/power down		150		200		250	ns
$t_{v(A)}$	Output data valid after address change	0		0		0		ns
t_{dis}	Output disable time from chip select or chip enable		100		100		100	ns

† All AC measurements are made at 10% and 90% points.

PARAMETER MEASUREMENT INFORMATION

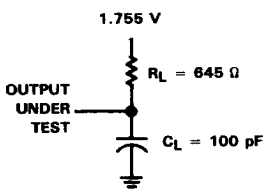


FIGURE 1. LOAD CIRCUIT

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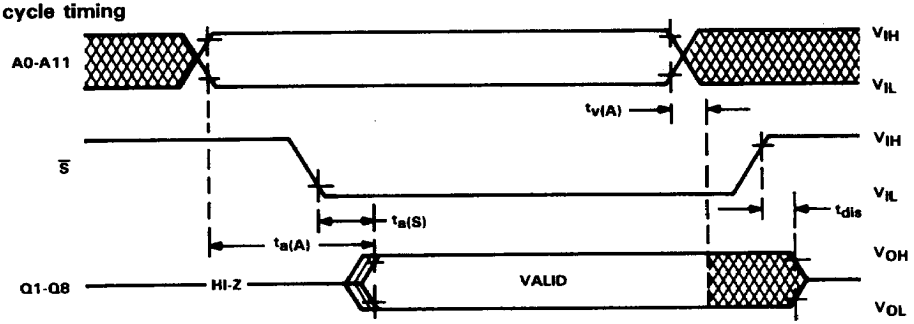
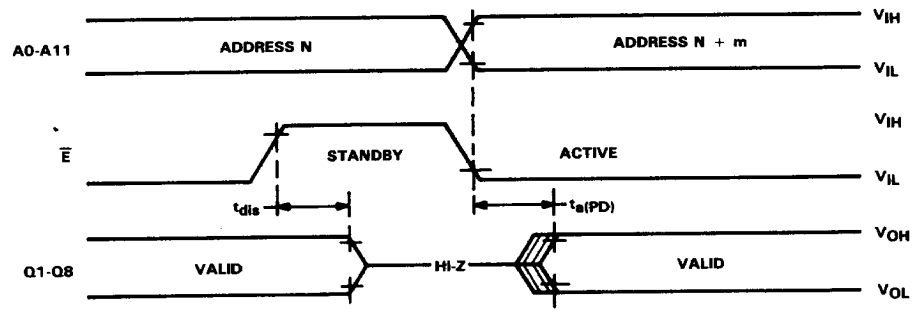
read cycle timing



standby mode



PROGRAMMING REQUIREMENTS AND CODE ACQUISITION

PROGRAMMING REQUIREMENTS: The TMS4732 is a fixed-program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer code inputs supplied. The device is organized as 4,096 8-bit words with address locations numbered 0 to 4,095. The 8-bit words can be coded as a 2-bit hexadecimal number between 00 and FF. Q1 is considered the least-significant bit and Q8 the most-significant bit. For addresses, A0 is the least-significant bit and A11 is the most-significant bit.

CODE ACQUISITION: The input media containing the customer programming data can be in the form of EPROMs, or data formatted in card images and transmitted via computer modem (contact TI for details on card image transmission). 32K EPROMS can be used to supply the customer data. In addition to the input media, the information requested in Table 1 is required at the same time in order to insure proper programming of device options and accurate data control.

TABLE 1. CUSTOMER/DEVICE INFORMATION

CUSTOMER: _____
SPECIFICATION NUMBER: _____
ROM CODE NAME: _____ ROM CODE CHECKSUM: _____

CUSTOMER PART NUMBER/SYMBOLIZATION:
CUSTOMER IS ALLOWED TWO (2) LINES OF UP TO
15 ALPHANUMERIC CHARACTERS PER LINE _____
_____

ADDRESS ACCESS TIME (SPEED): _____

PACKAGE TYPE: PLASTIC (N)_____

PIN OPTIONS: 1 = HIGH, 0 = LOW, PD = POWER DOWN, CS = CHIP SELECT

PIN 20: _____ PIN 21:_____ PD/CS:_____

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