Am1101A/1101A1

256-Bit Fully Decoded Random Access Memories

Distinctive Characteristics

- 256-bit fully decoded silicon gate MOS static random access memories.
- Typical access time: 650 ns Am1101A1
  850 ns Am1101A
- Chip select and OR tieable outputs allow easy expansion to large memories.
- 100% reliability assurance testing in compliance with MIL STD 883.

FUNCTIONAL DESCRIPTION

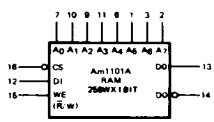
The Advanced Micro Devices' Am1101A and Am1101A1, are silicon gate MOS fully decoded random access 256-word by 1-bit memories. Low threshold silicon gate technology enables the devices to interface directly with standard DTL and TTL circuits. The memories use normally off P-channel MOS devices to form a static memory array that is ideal for use in small buffer memory applications. The Am1101A1 is a selected Am1101A for applications where higher speed is required and the Am1101ADM is a selected Am1101A which operates over the full military temperature range. The memories have an active LOW chip select input and OR tieable complementary outputs for ease of memory expansion. The chip select input can be driven by TTL MSI decoders such as the Am9301.

These memories are operated by applying DTL or TTL logic levels to the device inputs. For a read operation the chip select input, $\overline{CS}$, is held at a LOW logic level. The appropriate pattern is applied to the address inputs and the read/write input is held at a LOW logic level. The information stored in the addressed location is read out on complementary outputs, $\overline{DO}$ and DO, that can directly drive DTL or TTL circuitry. For a write operation, the chip select is held at a LOW logic level and the read/write input is moved to a HIGH logic level 300ns or more after the address has been selected and held HIGH for at least 400ns. This is to allow time for address decoding and to ensure writing data into the correct location. The data to be written into the addressed location must be present for at least 300ns before the end of the write command. During the write operation, if the chip is selected, the data outputs follow the data input line.

When the chip is unselected both the read/write and the data input leads are ineffective and both outputs go to a high impedance "OFF" state. The chip select, however, does not operate on the address decoders. This feature allows an effective increase in memory speed in some applications by using the faster delay from the chip select to the output.

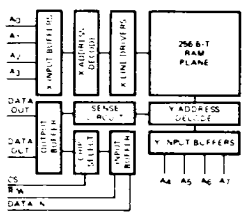
The memory can be operated in a low power standby mode by switching the periphery circuitry supply, V_{CC}, to V_{BB} and maintaining only the cell power supply, V_{DD}, supply current. When a chip is selected, the V_{CC} supply is separated from the V_{DD}. In this mode of operation the chip select and V_{CC} pin can be tied together, allowing full power to be dissipated only in selected chips and considerably reducing the system power in a large memory system.

LOGIC SYMBOL



V_{CC} = PIN 5
V_{DD} = PIN 8
V_{BB} = PIN 4

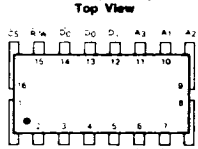
BLOCK DIAGRAM



Am1101A ORDERING INFORMATION

Package Type	Ambient Temperature Range	Order Number
Molded DIP	0°C to +75°C	P1101A
Hermetic DIP	0°C to +75°C	C1101A
Molded DIP	0°C to +75°C	P1101A1
Hermetic DIP	0°C to +75°C	C1101A1
Hermetic DIP	−55°C to +125°C	1101ADM

CONNECTION DIAGRAM
Top View



NOTE Pin 1 is marked for orientation.

MAXIMUM RATINGS Above which the useful life may be impaired (Note 1)

Storage Temperature	−65°C to +160°
Temperature (Case) Under Bias (Note 2)	−55°C to +125°
Power Dissipation at Room Temperature	700 m
All Input and Output Voltages with respect to the Most Positive Supply Voltage, V_{CC}	+0.3 V to −20
Supply Voltages V_{DD} and V_D with respect to V_{CC}	−20

OPERATING RANGE

Device	V_{CC}	V_D	V_{DD}	Temperature
1101A, 1101A1	+5.0 ±5%	−9.0 ±5%	−9.0 ±5%	0°C to +75°C
Am1101ADM	+5.0 ±5%	−10.0 ±5%	−10.0 ±5%	−55°C to +125°C

ELECTRICAL CHARACTERISTICS (over operating range unless otherwise specified)

		Am1101A, Am1101A1 (Note 3)			Am1101ADM (Note 3)			
Parameters	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
V_{OH} Output HIGH Voltage	$I_{OH} = -100\ \mu A$	3.5	4.9		3.5	4.9		Volts
V_{OL} Output LOW Voltage	$I_{OL} = -2.0$ mA			0.45				Volts
	$I_{OL} = -1.8$ mA						0.45	
V_{IH} (Note 4) Input HIGH Voltage		$V_{CC} -2$		$V_{CC} +0.3$	$V_{CC} -1$		$V_{CC} +0.3$	Volts
V_{IL} (Note 4) Input LOW Voltage		−10		$V_{CC} -4.5$	−10		$V_{CC} -4.5$	Volts
I_L Input Load Current	$V_{IN} = 0.0$ V		1.0	500		1.0	500	nA
I_{LO} Output Leakage Current	$V_{OUT} = 0.0$ V, $\overline{CS} = V_{IH}$ MIN.		1.0	500		1.0	500	nA
I_{OL} Output Sink Current	$V_{OUT} = 0.45$ V	2.0	8.0		1.8	8.0		mA
	$V_{OUT} = 0.45$ V, $T_A = +25°C$	3.0			3.0			
I_{OH} Output Source Current	$V_{OUT} = 0.0$ V	−2.0	−8.0		−1.8	−8.0		mA
	$V_{OUT} = 0.0$ V, $T_A = +25°C$	−3.0			−3.0			
I_{CEF} Output Clamp Current	$V_{OUT} = -1.0$ V		6	13		6	19	mA
I_{DD} DC Power Supply Current	$I_{OL} = 0.0$ mA, $T_A =$ MIN.			−16			−24	mA
	$I_{OL} = 0.0$ mA, $T_A = 25°C$		−9	−12		−11	−14	
I_D DC Power Supply Current	$I_{OL} = 0.0$ mA, $T_A =$ MIN.			−24			−35	mA
	$I_{OL} = 0.0$ mA, $T_A = 25°C$		−12	−18		−14	−21	
C_{IN} (Note 5) Input Capacitance	$V_{IN} = V_{CC}$, $f = 1$ MHz		7	10		7	10	pF
C_{OUT} (Note 5) Output Capacitance	$V_{OUT} = V_{CC}$, $f = 1$ MHz		7	10		7	10	pF
C_D (Note 5) Capacitance on V_D	$V_D = V_{CC}$, $f = 1$ MHz		20	35		20	35	pF

Note 1: Stresses above those listed in "MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation at these or at any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The thermal resistance θ_{CA} Case to Ambient is to a large extent dependent on ambient conditions such as velocity of air and the positions of packages and mounting boards relative to one another.

Note 3: Typical values are at normal voltage and $T_A = +25°C$

Note 4: A TTL device driving the memory must have its output HIGH $\geq V_{IH}$ min and its output LOW $< V_{IL}$ max even when driving other circuitry.

Note 5: This parameter is periodically sampled and not 100% tested.

SWITCHING CHARACTERISTICS (Over operating range unless otherwise noted)

(Output load is 1 TTL gate and 20 pF)

Parameters	Description		Conditions	Min.	Typ. (Note 1)	Max.	Units
$t_{pd}(A)$	Access Time, Address to Output HIGH or LOW	Am1101A	$\overline{CS}$ = L See Fig. 1	0.05	0.85	1.5	µs
		Am1101A1		0.05	0.65	1.0	µs
$t_{pd\ on}(\overline{CS})$	Delay, Chip Select to Output Active		Fig. 1	0.05	0.2	0.3	µs
$t_{pd\ off}(\overline{CS})$	Delay, Chip Select to Output HIGH Impedance State		Fig. 1	0.05	0.1	0.3	µs
$t_{pw}(\overline{CS})$	Minimum Chip Select Pulse Width (Note 2)		Fig. 2			0.4	µs
$t_{pw}(W)$	Minimum Write Pulse Width (Note 2)		Fig. 2			0.4	µs
$t_s(A)$	Address Set-Up Time		Fig. 2			0.3	µs
$t_h(A)$	Address Hold Time		Fig. 2			0.1	µs
$t_s(D)$	Data Set-Up Time		Fig. 2			0.3	µs
$t_h(D)$	Data Hold Time		Fig. 2			0.1	µs
T_R	System Read Cycle (defined by $t_{pd}(A)$	Am1101A	Fig. 1	1.5			µs
		Am1101A1		1.0			
T_W	System Write Cycle (defined by t_s max + t_{pw} max + t_h max			0.8			µs

Note 1: Typical speeds are at 25°C ambient.

Note 2: To write, $\overline{CS}$ and W must both be active for at least 400 ns; either signal can be used as a 400 ns "write pulse" if the other one is active during the writing period.

SWITCHING WAVEFORMS

CONDITIONS OF TEST:

Input pulse amplitudes: 0 to 5V, input pulse rise and fall time: 10 nsec. Speed measurements referenced to 1.5 V levels (unless otherwise noted). Output load is 1 TTL gate and C_L = 20 pF; measurements made at output of TTL gate ($t_{PD} \leq 10$ nsec).

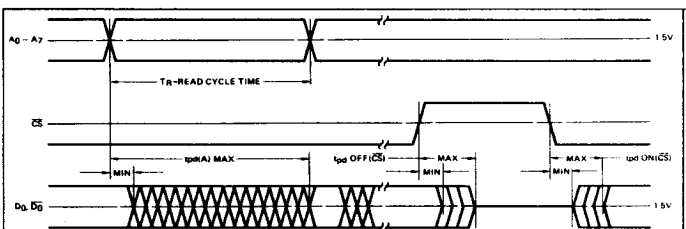


Fig. 1 READ CYCLE, showing access times for address and for chip select to and from the high impedance state.

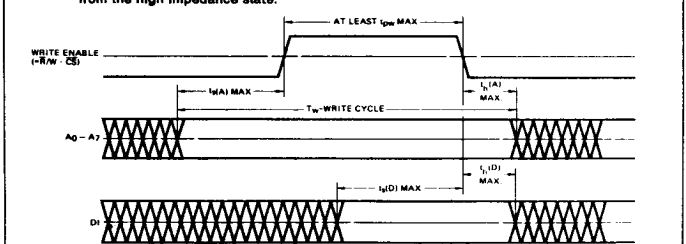


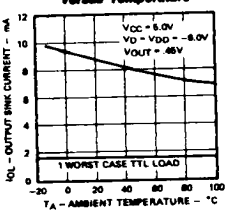
Fig. 2 WRITE CYCLE, showing required set-up times for address and data. The chip select and the write line are active. The data outputs will follow the data input during the write operation.

KEY TO TIMING DIAGRAM

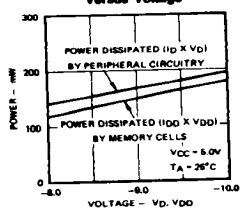
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

TYPICAL CHARACTERISTICS

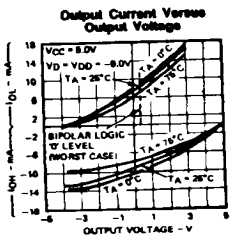
Output Sink Current Versus Temperature



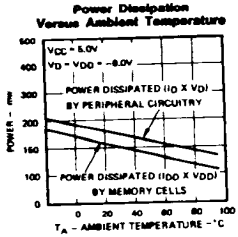
Power Dissipation Versus Voltage



Output Current Versus Output Voltage

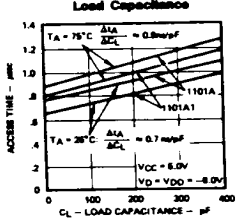


Power Dissipation Versus Ambient Temperature

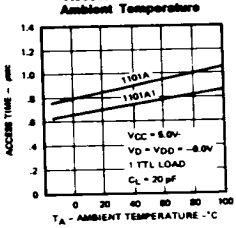


SWITCHING CHARACTERISTICS

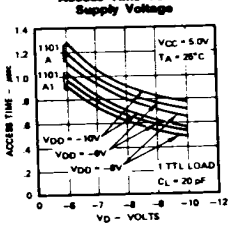
Access Time Versus Load Capacitance



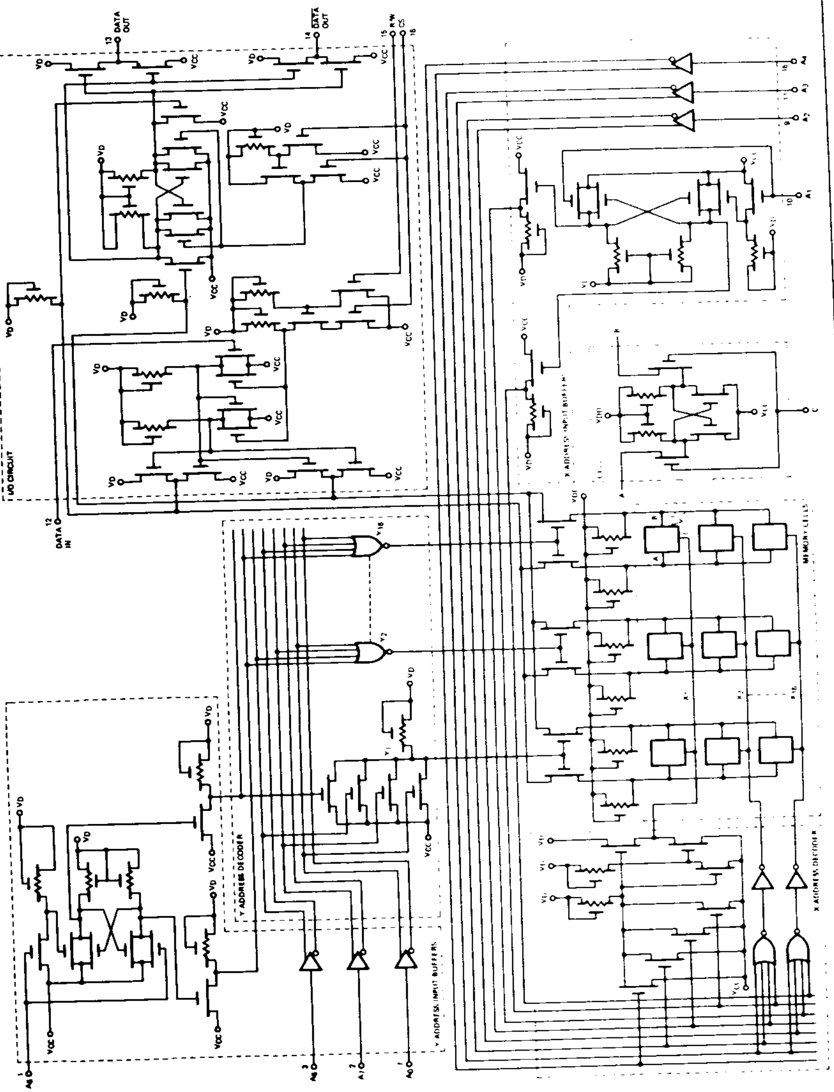
Access Time Versus Ambient Temperature



Access Time Versus Supply Voltage

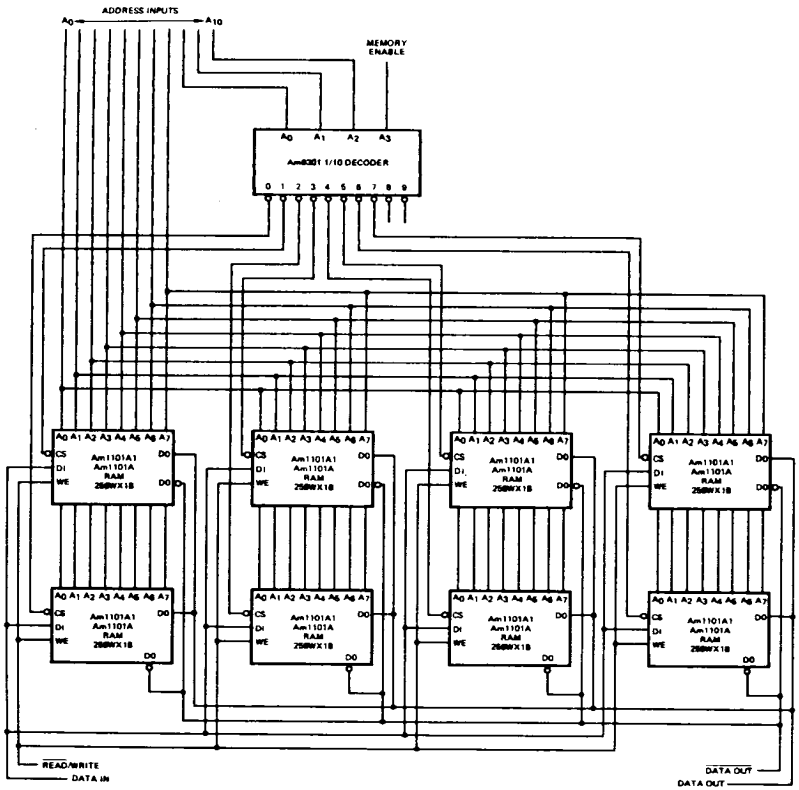


CIRCUIT DIAGRAM



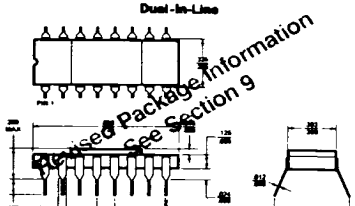
APPLICATION

2048 Word x 1 Bit Memory



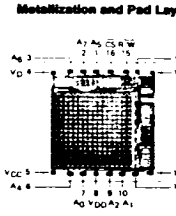
PHYSICAL DIMENSIONS

Dual-In-Line



Package Information
Refer to Section 9

Metallization and Pad Layout



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