Am27LS00/01 Series

256-Bit Low-Power Schottky Bipolar RAM

DISTINCTIVE CHARACTERISTICS

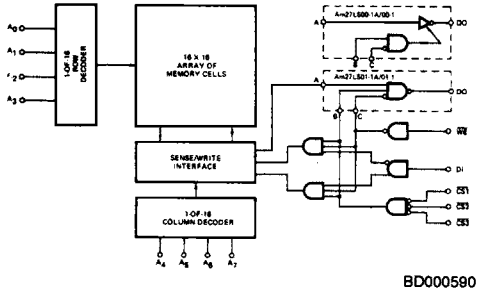
- High speed
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs or with open-collector outputs

GENERAL DESCRIPTION

The Am27LS00/01 Family is comprised of fully decoded bipolar random-access memories for use in high-speed buffer memories. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am27LS00 devices) or open-collector output (Am27LS01 devices). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output of the -1 device is active and inverts the value of DI (Write Transparent Operation). The other devices disable the output during the period $\overline{WE}$ is low. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

BLOCK DIAGRAM



BD000590

MODE SELECT TABLE

Input			Data Output Status $\overline{DO}$ (t_{n+1})	Mode
$\overline{CS}$	$\overline{WE}$	DI		
H	X	X	Output Disabled	No Selection
L	L	L	Inverted/Disabled*	Write '0'
L	L	H	Inverted/Disabled*	Write '1'
L	H	X	Selected Bit (Inverted)	Read

H = HIGH
L = LOW
X = Don't Care

*Inverted = -1 Devices
Disabled = All Other Devices

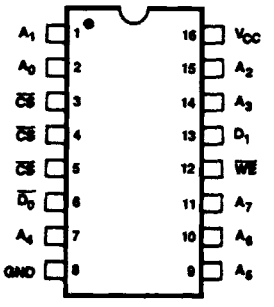
PRODUCT SELECTOR GUIDE

Open Collector Part Number	**STD**	Am27LS01A	Am27LS01	Am27LS01A	Am27LS01
	Write Transparent		Am27LS01-1		Am27LS01-1
Three-State Part Number	**STD**	Am27LS00A	Am27LS00	Am27LS00A	Am27LS00
	Write Transparent		Am27LS00-1		Am27LS00-1
Access Time		35 ns	45 ns		55 ns
Temperature Range		C	C	M	M

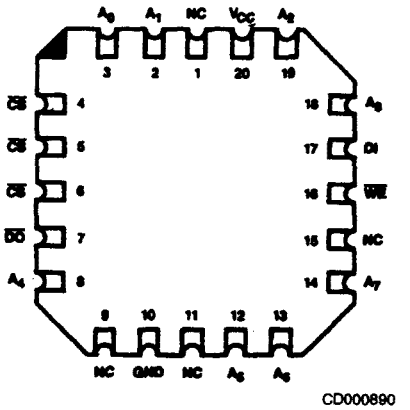
Publication # 03233 Rev. D Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

*



CD000880

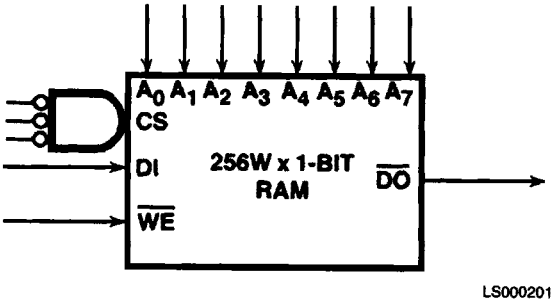


CD000890

*Same pinouts apply to both Ceramic DIP and Flatpack.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



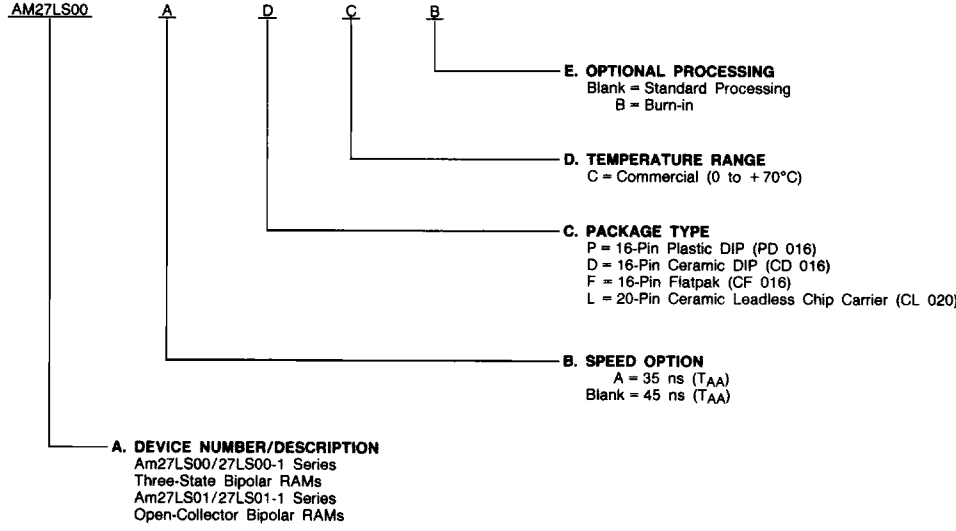
LS000201

V_{CC} = Power Supply
GND = Ground

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM27LS00	PC, PCB, DC, DCB, FC, FCB, LC, LCB
AM27LS00A	
AM27LS00-1	
AM27LS01	
AM27LS01A	
AM27LS01-1	

Valid Combinations

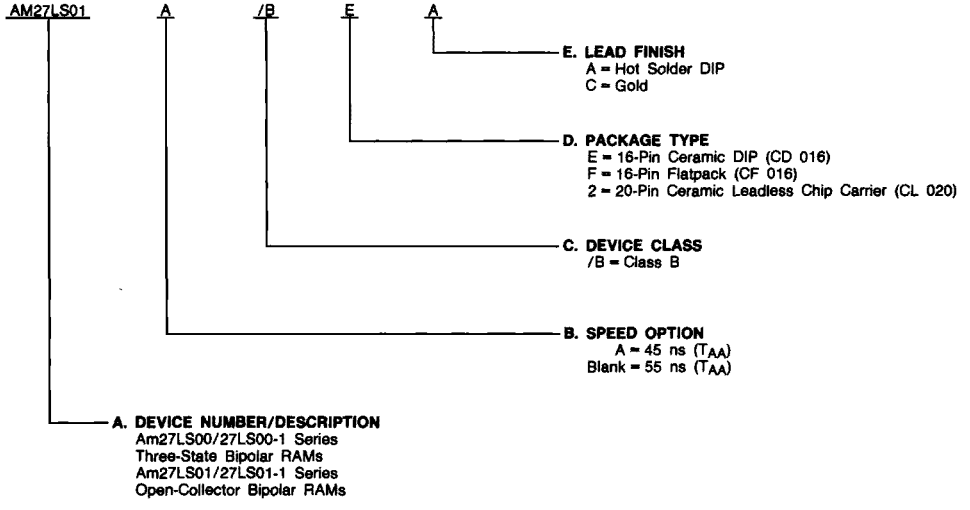
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

3

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27LS00	/BEA, /BFA, /B2C
AM27LS00A	
AM27LS00-1	
AM27LS01	
AM27LS01A	
AM27LS01-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage to ground potential
(Pin16 to Pin8) continuous ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
for High Output State ..... −0.5 V to+ V_{CC} max
DC Input Voltage ..... −0.5 V to +V_{CC}
Output Current, into Outputs ..... 30 mA
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0 to +75°C
Supply Voltage ..... +4.75 V to +5.25 V

Military (M) Devices
Temperature ..... −55 to +125°C
Supply Voltage ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

See Note 4

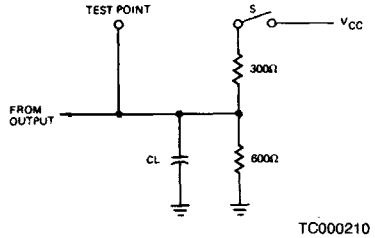
DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2 mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA			0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V				−0.030	−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				< 1	20	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V			−20	−30	−60	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.		"A" version		80	115	mA
				Standard		55	70	
V_{CL}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 2.4 V				0	30	μA
		$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0.4 V, V_{CC} = Max.		(Note 2)	−30	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Operating Specification with adequate time for temperatur e stabilization and transverse air flow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_C = T_J$ 0_JA = 44 − 59° c/w (with moving air) for ceramic DIPs.0_JC = 10 − 17° c/w for flatpack or leadless chip carriers.

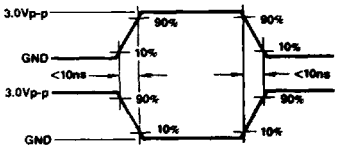
* See the last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST* CIRCUIT



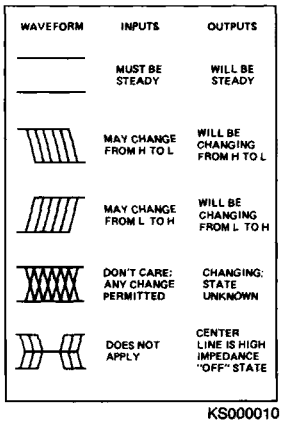
TC000210

SWITCHING TEST WAVEFORM



TW000030

KEY TO SWITCHING WAVEFORMS



KS000010

* See notes 3, 4, and 5 following Switching Characteristics table.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

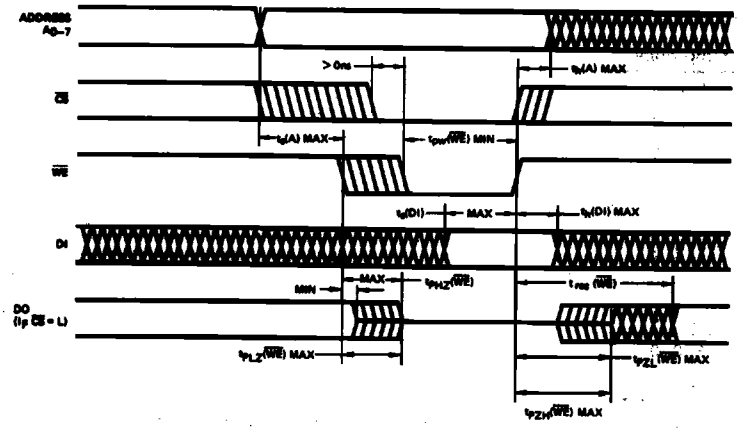
No.	Parameter Symbol	Parameter Description	Am27LS00A/01A Family				Am27S00/01 Family				Units
			C Devices		M Devices		C Devices		M Devices		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PLH}(A)	Delay from Address to Output		35		45		45		55	ns
2	t_{PHL}(A)										
3	$t_{PZH}(\overline{CS})$	Delay from Chip Select (LOW) to to Active Output and Correct Data		25		25		25		30	ns
4	$t_{PZL}(\overline{CS})$										
5	$t_{PZH}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data		35		45		45		55	ns
6	$t_{PZL}(\overline{WE})$										
7	t_s(A)	Setup Time Address (Prior to Initiation of Write)	0		5		0		5		ns
8	t_h(A)	Hold Time Address (After Termination of Write)	0		5		0		5		ns
9	t_s(DI)	Setup Time Data Input (Prior to Termination of Write)	25		30		30		35		ns
10	t_h(DI)	Hold Time Data Input (After Termination of Write)	0		5		0		5		ns
11	$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	25		30		30		35		ns
12	$t_{PHZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)		25		25		25		30	ns
13	$t_{PLZ}(\overline{CS})$										
14	$t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z) (Note 6)		30		40		30		40	ns
15	$t_{PHZ}(\overline{WE})$										

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. t_{PLH}(A) and t_{PHL}(A) are tested with S closed an d C_L = 50 pF with both input and output timing referenced to 1.5 V.
4. For open collector, all delays from write Enable($\overline{WE}$) o r Chip Select($\overline{CS}$) inputs to the Data Output(D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed and C_L = 50 pF and with both the input and output timing referenced to 1.5 V.
5. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S open, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed, C_L = 50 pF and with both the input and output timing referenced to 1.5 V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S open and $C_L \leq$ 5 pF and are measured between the 1.5 V level on the input and the V_{OH} – 500 mV level on the output. $T_{PLZ}(\overline{WE})$ and $T_{PLZ}(\overline{CS})$ are measured with S closed and $C_L \leq$ 5 pF and are measured between the 1.5 V level on the input and the V_{OL} + 500 mV level on the output.
6. Does not apply to –1 devices.

*See the last page of the spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS

WRITE MODE

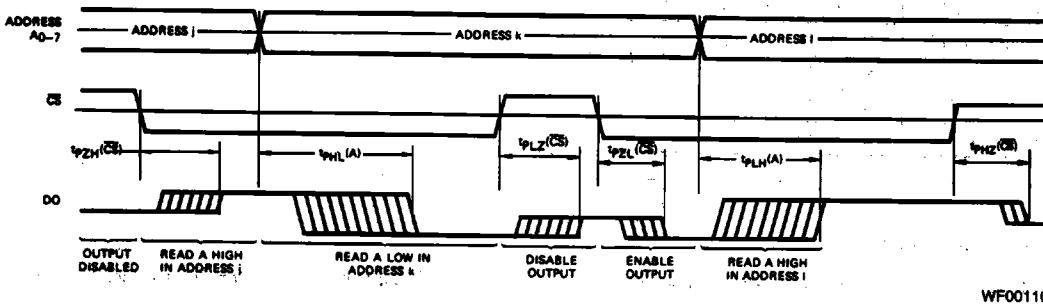


WF001091

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS00A/00) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

3

READ MODE



WF001100

Switching delays from address and chip select inputs to the data output. For the Am27LS00A/00, Am27LS00-1A/00-1 disabled output is "OFF," represented by a single center line. For the Am27LS01A/01, Am27LS01-1A/01-1, a disabled output is HIGH.

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
V_{CL}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups	Parameter Symbol	Subgroups
t_{PLH} (A)	9, 10, 11	t_s (DI)	9, 10, 11
t_{PHL} (A)	9, 10, 11	t_h (DI)	9, 10, 11
t_{PZH} ($\overline{CS}$)	9, 10, 11	t_{pw} ($\overline{WE}$)	9, 10, 11
t_{PZL} ($\overline{CS}$)	9, 10, 11	t_{PHZ} ($\overline{CS}$)	9, 10, 11
t_{PZH} ($\overline{WE}$)	9, 10, 11	t_{PLZ} ($\overline{CS}$)	9, 10, 11
t_{PZL} ($\overline{WE}$)	9, 10, 11	t_{PLZ} ($\overline{WE}$)	9, 10, 11
t_s (A)	9, 10, 11	t_{PHZ} ($\overline{WE}$)	9, 10, 11
t_h (A)	9, 10, 11		

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.