64-BIT BIPOLAR SCRATCH PAD MEMORY (16×4) 82S25 (O.C.), 3101A (O.C.), 54/74S189 (T.S.)

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

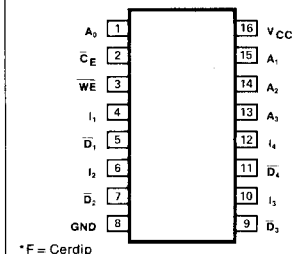
The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N74S189N, N82S25N, and for the military temperature range (-55°C to +125°C) specify S54S189 F or W, S82S25 F or W.

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION

F,N,W PACKAGE*



*F = Cerdip
N = Plastic
W = Flat Pak

TOP VIEW

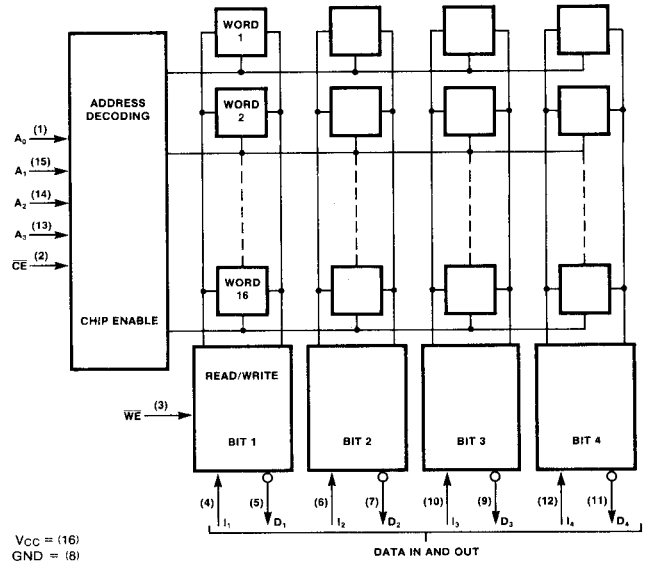
FEATURES

- **Output access time:**
  - **N82S25: 50ns max**
  - **S82S25: 60ns max**
  - **N3101A: 35ns max**
  - **N74S189: 35ns max**
  - **S54S189: 50ns max**
- **Power dissipation: 6.25mW/bit, typ**
- **Input loading:**
  - **N grade: -100μA max**
  - **S grade: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S25: Open collector**
  - **3101A: Open collector**
  - **54/74S189: Tri-state**
- **Schottky processed**
- **TTL compatible**

TRUTH TABLE

	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	54/74S189
				DATA OUT		
Read	0	1	X	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

BLOCK DIAGRAM



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AC ELECTRICAL CHARACTERISTICS

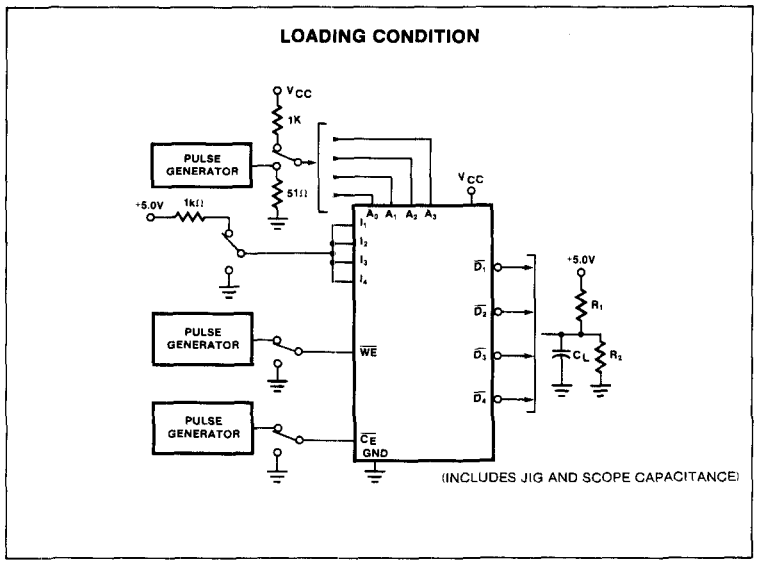
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $-55°C \le T_A \le +125°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	N82S25			S82S25			N3101A, N74S189			S54S189			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Access time															ns
T_{AA}	Address					50			60			35			50	
T_{CE}	Chip enable					35			35			17			25	
T_{CD}	Disable time	Output	Chip enable			35			35			17			40	ns
T_{WD}	Response time	Output	Write enable			25			30			25			50	ns
T_{WR}	Write recovery time					50			60			35			40	ns
	Setup and hold time															ns
T_{WSA}	Setup time	Write enable	Address	5			10			0			0			
T_{WHA}	Hold time			5			10			0			10			
T_{WSD}	Setup time	Write enable	Data in	30			30			25			30			
T_{WHD}	Hold time			5			10			0			10			
T_{WSC}	Setup time	Write enable	$\overline{CE}$	0			0			0			0			
T_{WHC}	Hold time			5			5			0			0			
	Pulse width															ns
T_{WP}	Write enable[5]			30			30			25			30			

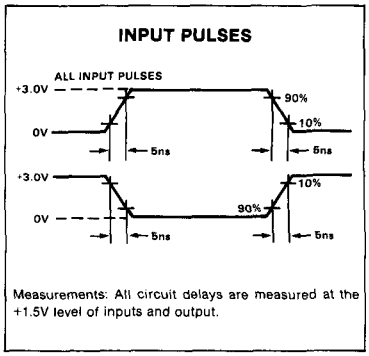
NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: high ≈ +5.0V, low ≈ GND.
7. Test each input one at a time.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage High	+5.5	Vdc
T_A	Temperature range Operating		°C
	N grade	0 to +75	
	S grade	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[7]		TEST CONDITIONS[6]	N GRADE			S GRADE			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,7]	I_{IN} = −12mA, V_{CC} = Min			−1.5			−1.5	
	Output voltage	$\overline{CE}$ = Low							V
V_{OL}	Low[2,3,1]	I_{OUT} = 16mA, V_{CC} = Min			0.45			0.5	
V_{OH}	High (54/74S189)[1]	I_{OUT} = 2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			10			25	
	Output current								
I_{OLK}	Leakage	$\overline{CE}$ = high, V_{OUT} = 5.5V, V_{CC} = Min			100			100	μA
I_{OS}	Short circuit (54/74S189)	$\overline{CE}$ = Low V_{OUT} = 0V			−100	−30		−100	mA
$I_{O(OFF)}$	Hi-Z (54/74S189)	2.4 ≥ V_{OUT} ≥ 0.4V			±50			±50	μA
I_{CC}	Supply current[3]								mA
	82S25				105			120	
	3101A				105			120	
	54/74S189				110			110	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V, $\overline{CE}$ = high		8			8		

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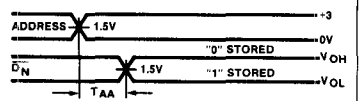
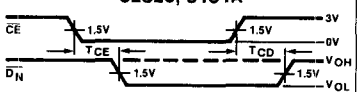
TIMING DIAGRAMS

READ CYCLE



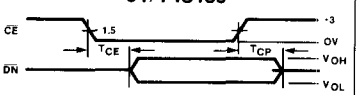
Address Access Time

82S25, 3101A



Chip Enable/Disable Times
Open Collector

54/74S189



Chip Enable/Disable Times
Tri-State

WRITE CYCLE