Am2102/Am2102-1/Am2102-

1024-Bit Static N-Channel RAM

Distinctive Characteristics

- Operates from single 5V power supply
- Three speed selections: 1μsec, 650ns, 500ns
- All inputs and outputs directly TTL compatible
- No clocks required
- 100% reliability testing in accordance with MIL-STD-883

FUNCTIONAL DESCRIPTION

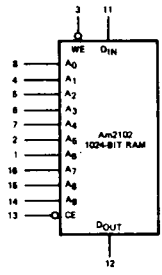
The Am2102 is a static N-channel 1024-bit random access memory. The device operates from a single +5 volt power supply and all inputs and outputs are directly TTL compatible with no external components required. The memory is addressed for reading or writing one bit by applying a binary code to the 10 address inputs A_0–A_9. Writing is accomplished by lowering the write enable ($\overline{WE}$) and the chip select ($\overline{CE}$); the data on the data input (D_{in}) will be stored in the addressed location. If the chip select is lowered while write enable is HIGH, then the data stored in the addressed location will be read out on the data output (D_{out}).

Any time the chip select is HIGH, the entire chip is disabled. Data cannot be written into the memory and the output will go to a high impedance OFF state. When chip select is LOW, the output will drive at least one TTL load in both the HIGH and LOW states. During the write operation, the data output follows the data input.

The chip select function and the three-state output make the construction of a large array using Am2102 chips very easy. Am2102 inputs and outputs can be tied together and chips selected by a standard TTL decoder such as the Am9321 or Am9301.

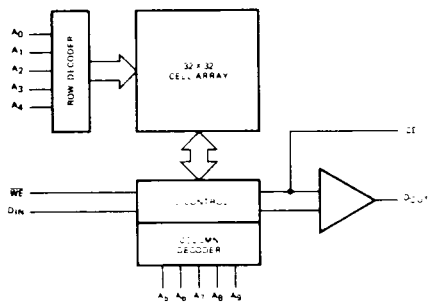
The Am2102 is available in three different cycle time selections. The Am2102 operates with a 1μsec minimum read or write cycle, the Am2102-1 requires a 500ns minimum read or write cycle, and the Am2102-2 requires a 650ns minimum read or write cycle.

LOGIC SYMBOL



V_{CC} = Pin 10
GND = Pin 9

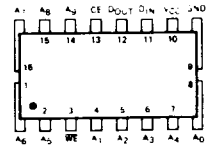
BLOCK DIAGRAM



Am2102 ORDERING INFORMATION

Package Type	Ambient Temperature Range	1μsec Order Number	500ns Order Number	650ns Order Number
Molded DIP	0°C to +70°C	P2102	P2102-1	P2102-2
Hermetic DIP	0°C to +70°C	C2102	C2102-1	C2102-2

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +70°C
Supply Voltage to Ground Potential (Pin 10 to Pin 9) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs	−0.5V to +7V
DC Input Voltage	−0.5V to +7V

OPERATING RANGE

Part Number	V_{CC}	Ambient Temperature
Am2102, Am2102-1, Am2102-2	5.0V ±5%	0°C to +70°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −100µA		2.2			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 1.9mA				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.2		V_{CC}	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		−0.5		0.65	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., V_{IN} = 0V to 5.25 V				10	µA
I_{CC1}	Power Supply Current	All inputs = V_{CC} Data out open V_{CC} = MAX.	T_A = 25°C		30	60	mA
I_{CC2}			T_A = 0°C to +70°C		30	70	
I_{LO}	Output Leakage Current	$V_{\overline{CE}}$ = 2.2V	V_{OUT} = 4.0V			10	µA
			V_{OUT} = 0.45V			−100	

Note 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C

CAPACITANCE (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance, Any Input	V_{IN} = 0V, f = 1MHz		3	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1MHz		7	10	pF

Am2102 SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS (T_A = 0°C to 70°C, V_{CC} = 5V±5%)

Load = 1 TTL Gate and 100 pF, V_{IL} = 0.65V, V_{IH} = 2.2V, t_r = t_f = 20ns

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{RC}	Read Cycle Time		1000			ns
t_A	Access Time			500	1000	ns
t_{CO}	$\overline{CE}$ LOW to Output				500	ns
t_{OH1}	Previous Read Data Valid with Respect to Address		50			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Select		0			ns
t_{WC}	Write Cycle Time		1000			ns
t_{AW}	Address Set-Up Time		200			ns
t_{WP}	Write Pulse Width		750			ns
t_{WR}	Write Recovery Time		50			ns
t_{DW}	Data Set-Up Time		800			ns
t_{DH}	Data Hold Time		100			ns
t_{CW}	Chip Enable Hold Time		900			ns

Am2102-1 SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS (T_A = 0°C to 70 $_C$ = 5V±5%)

Load = 1 TTL Gate and 100 pF, V_{IL} = 0.65V, V_{IH} = 2.2V, t_r = t_f = 20ns

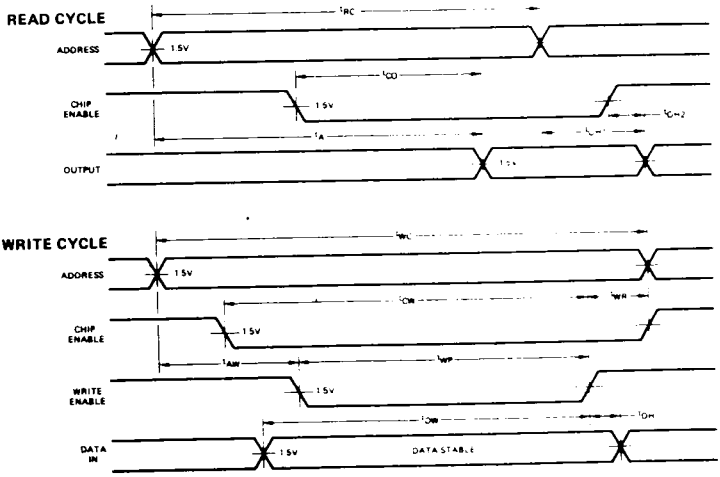
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{RC}	Read Cycle Time		500			ns
t_A	Access Time				500	ns
t_{CO}	$\overline{CE}$ LOW to Output				350	ns
t_{OH1}	Previous Read Data Valid with Respect to Address		50			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Select		0			ns
t_{WC}	Write Cycle Time		500			ns
t_{AW}	Address Set-Up Time		150			ns
t_{WP}	Write Pulse Width		300			ns
t_{WR}	Write Recovery Time		50			ns
t_{DW}	Data Set-Up Time		330			ns
t_{DH}	Data Hold Time		100			ns
t_{CW}	Chip Enable Hold Time		400			ns

Am2102-2 SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS (T_A = 0°C to 70°C, V_{CC} = 5V±5%)

Load = 1 TTL Gate and 100 pF, V_{IL} = 0.65V, V_{IH} = 2.2V, t_r = t_f = 20ns

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{RC}	Read Cycle Time		650			ns
t_A	Access Time				650	ns
t_{CO}	$\overline{CE}$ LOW to Output				400	ns
t_{OH1}	Previous Read Data Valid with Respect to Address		50			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Select		0			ns
t_{WC}	Write Cycle Time		650			ns
t_{AW}	Address Set-Up Time		200			ns
t_{WP}	Write Pulse Width		400			ns
t_{WR}	Write Recovery Time		50			ns
t_{DW}	Data Set-Up Time		450			ns
t_{DH}	Data Hold Time		100			ns
t_{CW}	Chip Enable Hold Time		550			ns

SWITCHING WAVEFORMS



DEFINITIO TERMS

FUNCTIONAL TERMS

$\overline{CE}$ Active LOW chip enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW write enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drains are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH1} Minimum Access Time. Minimum time which will elapse between change of address and any change on the data output.

t_{OH2} Minimum time which will elapse between a change on the chip enable and any change on the data output.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-Up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

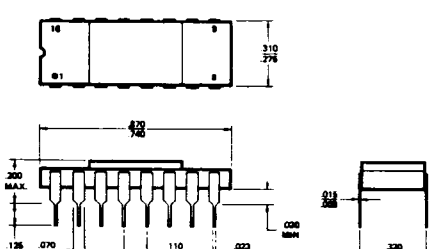
t_{DW} Data Set-Up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

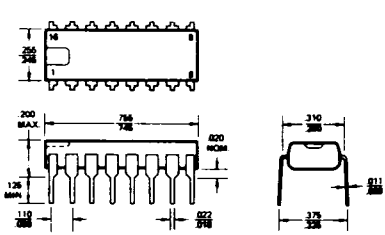
t_{CW} Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

PHYSICAL DIMENSIONS
Dual-In-Line

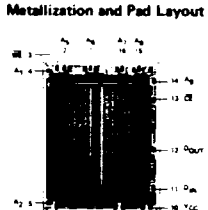
16-Pin Side Brazed



16-Pin Molded



Metallization and Pad Layout



DIE SIZE 0.126" X 0.164"

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

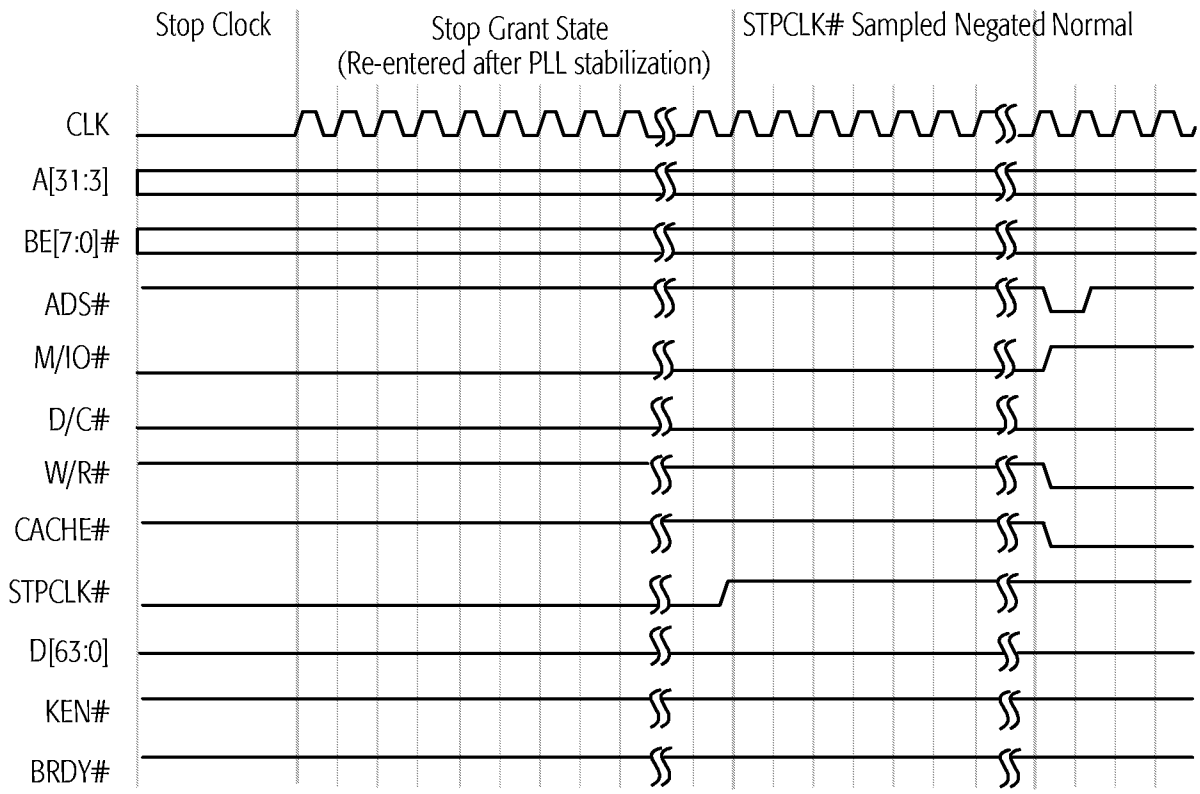


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

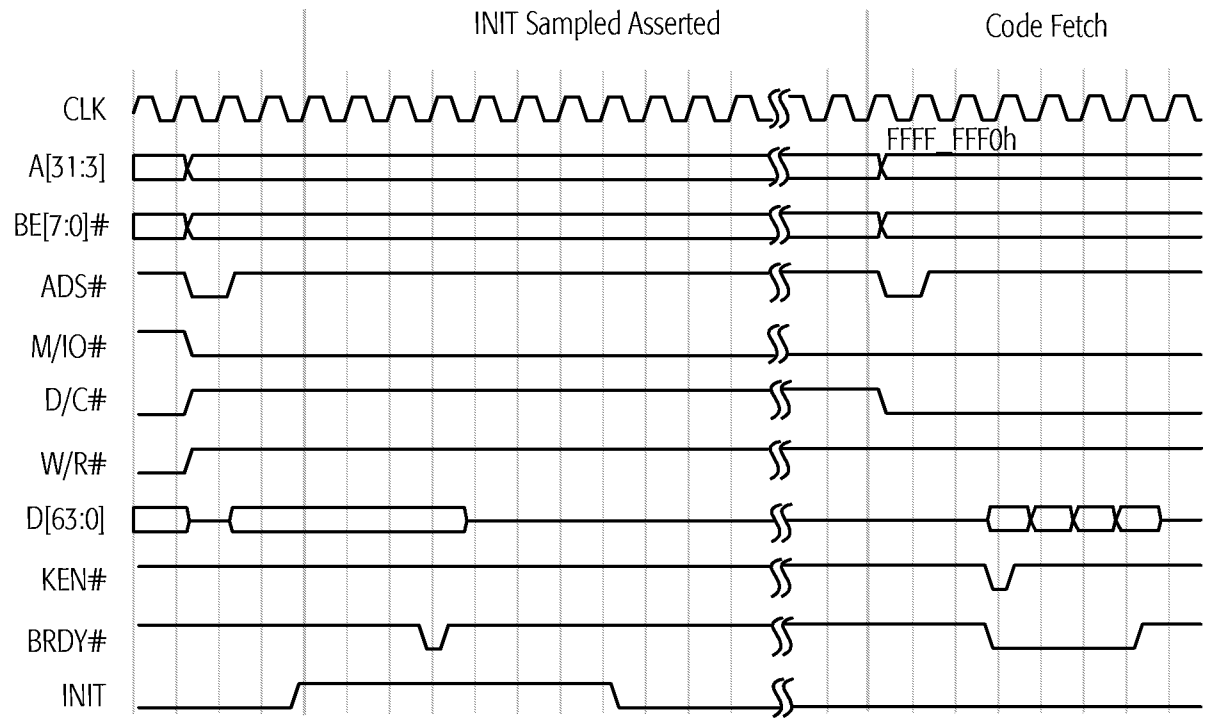


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.