2104A FAMILY
4096 x 1 BIT DYNAMIC RAM

	2104A-1	2104A-2	2104A-3	2104A-4
Max. Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	320	375	375	425
Max. IDD (mA)	35	32	30	30

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM: 462mW Operating 27mW Standby**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on All Power Supplies +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **$\overline{RAS}$-Only Refresh Operation**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

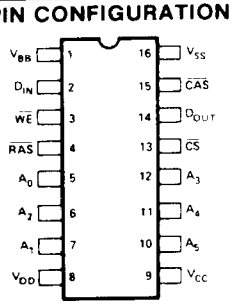
The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

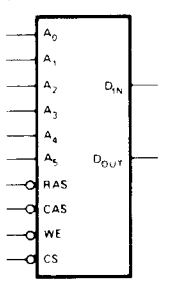
A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a $\overline{RAS}$-only refresh cycle or read cycle at each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for page mode operation, $\overline{RAS}$-only refresh, and $\overline{CAS}$-only deselect.

PIN CONFIGURATION



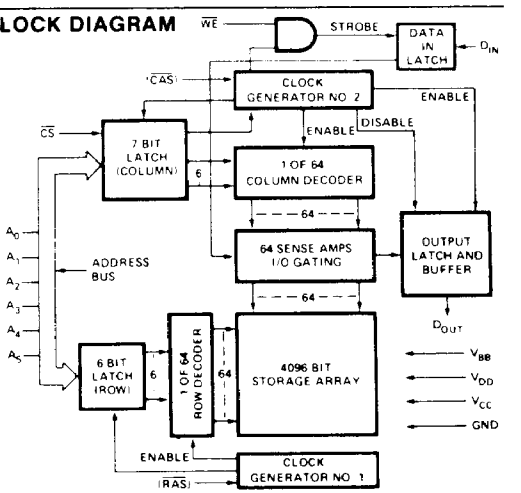
LOGIC DIAGRAM



PIN NAMES

A_0 A_5	ADDRESS INPUTS	WE	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4.5V) . . . . . -0.3V to +20V
Power Dissipation 1.0W
Data Out Current . . . . . 50 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0° to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = V_{SS} to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH}; V_{OUT} = 0 to 5.5V
I_{DD1}[3]	V_{DD} Standby Current		0.7	2	mA	V_{DD} = 13.2V; $\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected prior to measurement. See Note 5.
			0.7	1.5	mA	V_{DD} = 12.6V
I_{BB1}	V_{BB} Standby Current		5	50	µA	V_{DD} = 13.2V
I_{DD2}[3]	Operating V_{DD} Current		24	35	mA	2104A-1; t_{RC} = $t_{RC\ MIN}$
			22	32	mA	2104A-2; t_{RC} = $t_{RC\ MIN}$
			20	30	mA	2104A-3, 2104A-4; t_{RC} = $t_{RC\ MIN}$
I_{BB2}	Operating V_{BB} Current		130	325	µA	Min cycle time. T_A = 0°C
I_{CC1}[4]	V_{CC} Supply Current when Deselected			10	µA	
I_{DD3}	Operating V_{DD} Current ($\overline{RAS}$-only cycle)		12	25	mA	2104A-1, 2104A-2; t_{RC} = $t_{RC\ MIN}$
			10	22	mA	2104A-3, 2104A-4; t_{RC} = $t_{RC\ MIN}$
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V	
V_{IH}	Input High Voltage (any input)	2.4		7.0	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA

CAPACITANCE[6] T_A = 25°C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance (A_0-A_5, D_{IN}, $\overline{CS}$)	3	7	pF	V_{IN} = V_{SS}
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{WRITE}$)	3	7	pF	V_{IN} = V_{SS}
C_O	Output Capacitance (D_{OUT})	4	7	pF	V_{OUT} = 0V
C_{I3}	Input Capacitance ($\overline{CAS}$)	6	7	pF	V_{IN} = V_{SS}

Notes: 1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C.CHARACTERISTICS[1,2]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Time Between Refresh		2		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		120		125		ns
t_{CP}	$\overline{CAS}$ Precharge Time	60		80		110		110		ns
t_{RCD}[3]	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	80	135	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		165		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	95		120		160		215		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	-10		-10		-10		-10		ns
t_{RAH}	Row Address Hold Time	20		25		35		80		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	45		55		75		80		ns
t_T	Rise or Fall Time	3	50	3	50	3	50	3	50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	60	0	60	0	80	ns
t_{CAC}[4,5]	Access Time From $\overline{CAS}$		100		135		165		165	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		150		200		250		300	ns

READ CYCLE

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		375		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	300	10000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		135		165		165		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		ns
t_{DOH}	Data Out Hold Time	10		10		10		10		μs

WRITE CYCLE

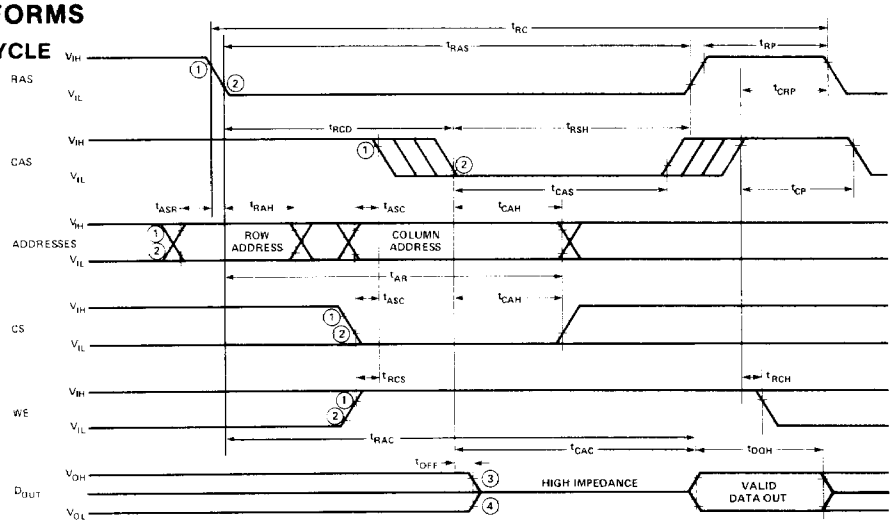
Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		375		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	300	10000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		135		165		165		ns
t_{WCS}[6]	Write Command Set-Up Time	0		0		0		0		ns
t_{WCH}	Write Command Hold Time	45		55		75		80		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	50		70		85		130		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		130		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		65		75		80		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns

NOTES:

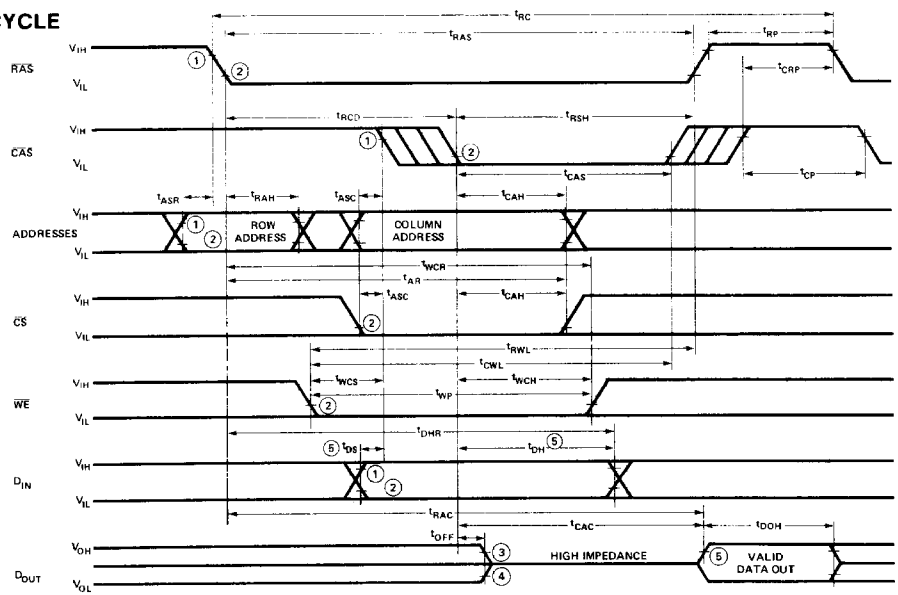
1. All voltages referenced to V_{SS}.
2. A.C. Characteristics assume t_T = 5ns.
3. $t_{RCD(MAX)}$ is specified as a reference point only; if $t_{RCD} \leq t_{RCD(MAX)}$ access time is t_{RAC}, if $t_{RCD} > t_{RCD(MAX)}$ access time is $t_{RCD} + t_{CAC}$.
4. Load = 2 TTL loads and 100pF.
5. Assumes $t_{RCD} \geq t_{RCD(MAX)}$.
6. In a write cycle with $t_{WCS} \geq t_{WCS(MIN)}$ the cycle is an early write cycle and D_{OUT} will be data written into the selected cell ($D_{OUT} = D_{IN}$). If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$ the cycle is a read-modify-write cycle and D_{OUT} will be data from the selected address read. If neither of the above conditions are satisfied, D_{OUT} is indeterminate.

WAVEFORMS

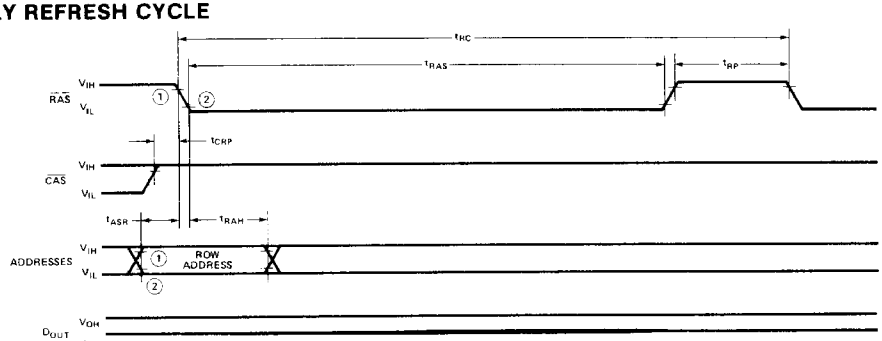
READ CYCLE



WRITE CYCLE



RAS-ONLY REFRESH CYCLE



(See next page for notes)

A.C.CHARACTERISTICS[7,8]

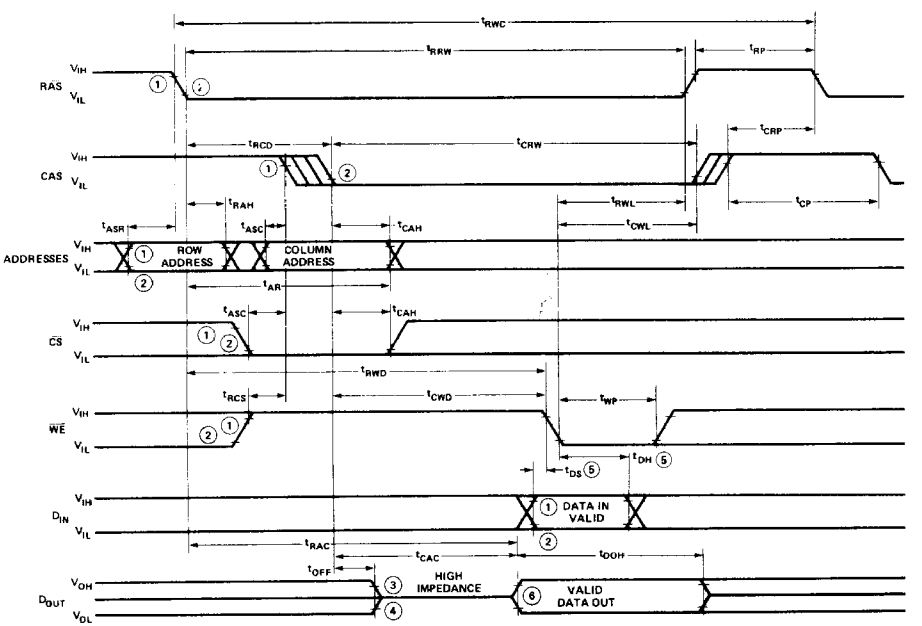
T_A = 0° to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2104A-1 Min.	2104A-1 Max.	2104A-2 Min.	2104A-2 Max.	2104A-3 Min.	2104A-3 Max.	2104A-4 Min.	2104A-4 Max.	Unit
t_{RWC}	Read Modify Write Cycle Time[2]	330		420		480		575		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	115		155		180		250		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	165	10,000	220	10,000	265	10,000	385	10,000	ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	50		70		85		130		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		130		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RWD}[6]	$\overline{RAS}$ to $\overline{WE}$ Delay	110		145		175		250		ns
t_{CWD}[6]	$\overline{CAS}$ to $\overline{WE}$ Delay	60		80		90		115		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		65		75		80		ns

WAVEFORMS

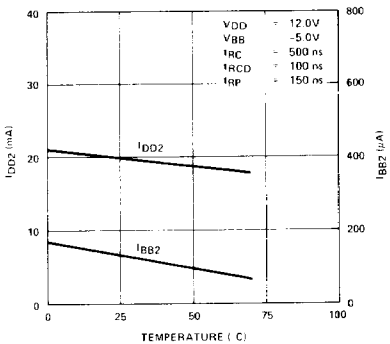
READ-MODIFY-WRITE CYCLE



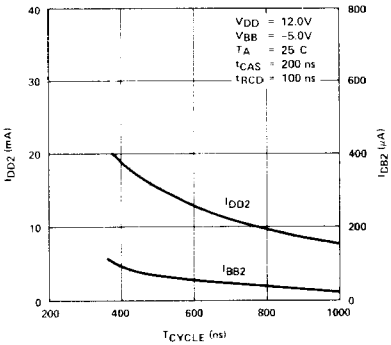
Notes: 1,2. V_{IHMIN} or V_{IHCMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. Referenced to CAS or WE, whichever occurs last.
6. In a write cycle with $t_{WCS} \geq t_{WCS(MIN)}$ the cycle is an early write cycle and D_{OUT} will be data written into the selected cell ($D_{OUT} = D_{IN}$). If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$ the cycle is a read-modify-write cycle and D_{OUT} will be data from the selected address read. If neither of the above conditions are satisfied, D_{OUT} is indeterminate.
7. All voltages referenced to V_{SS}.
8. A.C. Characteristics assume t_T = 5ns.

TYPICAL CHARACTERISTICS

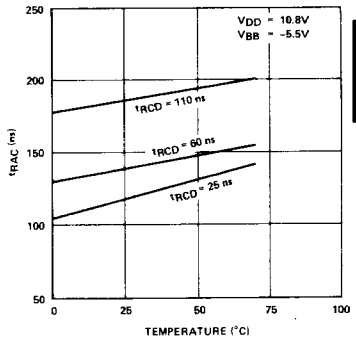
TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE



TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME



TYPICAL ACCESS TIME VS. TEMPERATURE



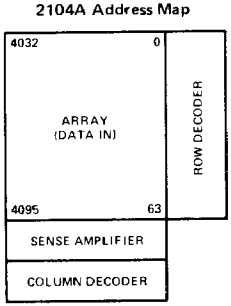
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0" corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid for at least $t_{DOH\ MAX}$. A subsequent $\overline{CAS}$ must be given to the device either by a Read, Write, Read-Modify-Write, $\overline{CAS}$-only or $\overline{RAS}$/$\overline{CAS}$ refresh cycle.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. $\overline{RAS}$ to $\overline{CAS}$ delay time, t_{RCD}, is a system dependent timing parameter. For example, substituting the device parameters to the 2104A-4 yields:

3. $t_{ACC} = t_{RAC} = 300ns$ for $80nsec \leq t_{RCD} \leq 135nsec$

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 165ns$ for $t_{RCD} > 135ns$.

Note that if 80nsec ≤ t_{RCD} ≤ 135nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If t_{RCD} > 135ns, access time is determined by equation 4. This 55ns interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCD} skew is designed in at the device level to allow minimum access times to be achieved in practical system designs.

WRITE CYCLE

A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ but t_{CWD} < $t_{CWD\ MIN}$ and t_{RWD} < $t_{RWD\ MIN}$, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

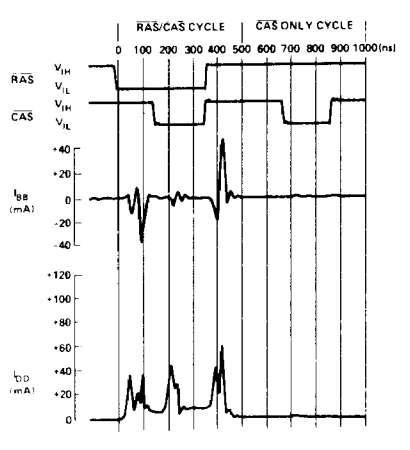
A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low during a selected $\overline{RAS}/\overline{CAS}$ cycle with $t_{RWD} \geq t_{RWD\ MIN}$ and $t_{CWD} \geq t_{CWD\ MIN}$. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read from the selected cell and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}/\overline{CAS}$ cycle was being performed.

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.



TYPICAL SUPPLY CURRENTS VS TIME

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any cycle (Read, Write, Read-Modify-Write, $\overline{RAS}$-only refresh) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}/\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

PAGE MODE OPERATION

The 2104A is designed for page mode operation. Product tested to page mode operating specifications are available upon request.

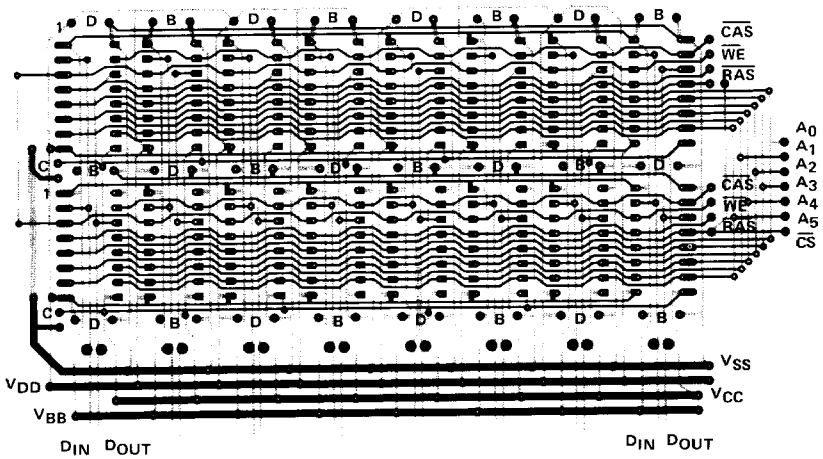
POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}/\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}