BPK 5V74
4MBIT BUBBLE MEMORY SUBSYSTEM

BPK 5V74-4	10°C To 55°C

- **4 Mbit (512K Bytes) Non-Volatile, Solid-state, Read/Write Bubble Memory Subsystem**
- **Interfaces to Host Microprocessor Via Additional Bubble Memory Controller**
- **Contains Bubble Memory and ICs for Production with 4Mbit Bubble Memory**
- **Modularity Provides Expansion Up to Eight Subsystems Per Controller**
- **Maximum Data Rate of 200K bit/sec with One Subsystem**
- **Maximum Data Rate of 1.6M bit/sec with Eight Subsystems in Parallel and Time Multiplexed**
- **Average Random Access Time of 88 ms**
- **Bubble Memory in Leaded Package**

The BPK 5V74 Bubble Memory Subsystem is a modular building block used to design bubble memory systems. In a complete bubble memory system, an 7224 Bubble Memory Controller (BMC) interfaces the BPK 5V74 subsystem to the host processor.

The modular Intel subsystem provides a path for density expansion. One BMC can interface up to eight 4 Mbit subsystems. Thus, a 4 MBit (512 KByte) system can be expanded up to a 32 MBit system by adding subsystems. BMC's can be combined in parallel to further expand the system memory capacity.

Together, the BPK 5V74 Bubble Storage Subsystem and a 7224 controller provide a reliable mass storage system for any application. This bubble memory system can be customized to the particular layout and form factor of many different systems.

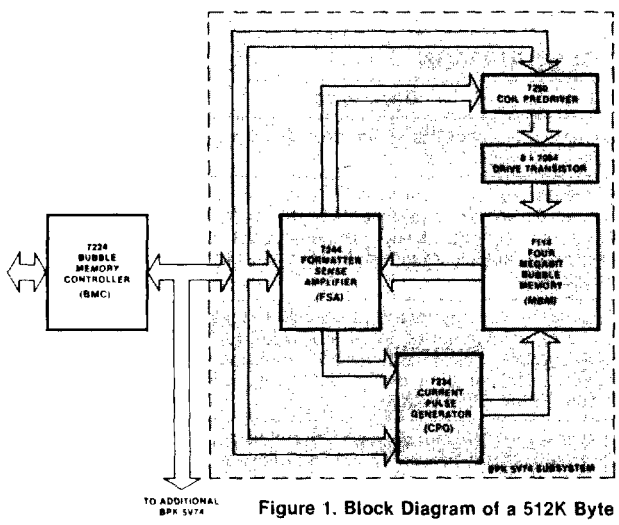

Figure 1. Block Diagram of a 512K Byte Bubble Storage System

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FUNCTIONAL DESCRIPTION

An BPK 5V74 subsystem and a 7224 controller comprise a complete bubble memory system. The 4 MBit BMC, the 7224, provides the interface between the host microprocessor and the bubble memory subsystem and provides all the timing and control signals to the subsystem. The user interface of the BMC is compatible with microprocessor bus systems for 8080, 8085, 8086, 8088, 80186, 80286 and other standard microprocessors. The BMC is a software driven device utilizing 18 convenient commands. The design engineer's primary responsibility is interfacing to the BMC. This is comparable to interfacing a disk drive controller.

The BPK 5V74 consists of one 4 MBit Magnetic Bubble Memory (MBM) and additional support IC's (see Figure 1). These are the basic components to build a non-volatile, solid-state, read/write military memory system utilizing 4 MBit bubble memory. The bubble memory is in a leaded package. The complete family of LSI support circuits has been designed to handle the complex analog interface associated with bubble devices. The immediate support circuitry for the MBM consists of — an 7250 Coil Predriver (CPD), eight 7264 MOS FETs Transistor Packs, an 7234 Current Pulse Generator (CPG), and an 7244 Formatter/Sense Amplifier (FSA).

Data integrity is insured by the automatic error correction designed into the BPK 5V74.

The average random access time of a 4 MBit subsystem is 88 ms with a 200Kbit/sec maximum data transfer rate. Operating several subsystems in parallel, the BMC uses time division multiplexing. Therefore, the maximum data rate increases correspondingly for the whole system.

Operating subsystems serially, one MBM being accessed at a time, the maximum data transfer rate is still 200Kbit/sec. If low power consumption is a critical design goal, the bubble memory subsystem can be powered down when it is not being accessed, thus reducing the average power consumption.

The data in the 4 Mbit subsystem is organized in 8192 pages, each with 64 bytes. Conceptually, the data organization with pages is analogous to a disk system's sectors. In system's with multiple bubble memories, the page size can vary from 64 bytes to 512 bytes depending on the number of subsystems and if the subsystems are operating in parallel or serially, being accessed one at a time.

The BPK 5V74 subsystem has matched components. Each of the components in the subsystem is described in more detail in the rest of this data sheet.

BPK 5V74 FUNCTIONAL DESCRIPTION

Item	Description	Part Number
4 MBit Bubble Memory	20-pin leaded package which provides 4 megabit of non-volatile storage.	7114
Current Pulse Generator	Converts digital timing signals to analog current pulses suited to the drive requirements of the MBM. The CPG provides the replicate, swap, generate, boot replicate, and bootswap pulses required by the MBM. 22 Pin DIP Package.	7234
Dual Formatter/Sense Amp	Provides direct interface to the Bubble Memory. The FSA contains on-chip sense amplifiers, a full FIFO data block buffer, burst error detection and correction circuits, and circuitry for handling of the bubble memory redundant loops. 20 Pin DIP package.	7244
Coil Predriver	Provides the high voltage, high current outputs to drive the Quad VMOS transistors. 16 Pin DIP package.	7250
VMOS Coil Drive Transistors (8)	Switches the required current to drive the X and Y coils of the Bubble Memory. 3 Pin Discrete.	7264

For additional packaging information see the packaging information section.

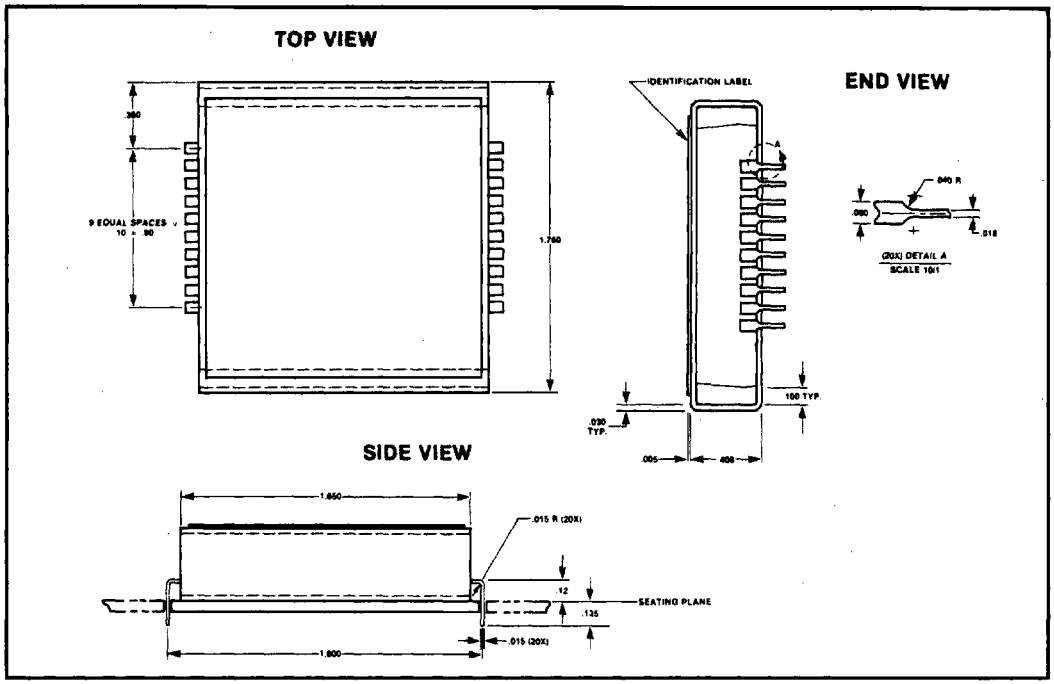


Figure 2. 4MBit Leaded Bubble Memory Package

BPK 5V74 TEMPERATURE RANGE

Bubble Memory Temperature Ranges		Support Circuits Min. Operating Temperature	Description
Operating	Non-Volatile Storage		
10° to 55°C Case	−20 to +75°C	10° to +55°C Ambient	4 Mbit Bubble Storage Sub-System

SPECIFICATIONS

Capacity

512K Byte per BPK 5V74
Maximum of 8 BPK 5V74 per 7224 Controller

Performance

Avg. Access Time . . . . . 88 msec

Data Organization

64 bytes per page
8192 pages per BPK 5V74

Addressing Scheme

Logical page number

Environmental

Temperature: See Ordering Information
Operating Humidity: 0—95% Non-Condensing

DATA TRANSFER RATES (Examples of System Configurations)

Parameter	One BPK 5V74 Unit	Four BPK 5V74 Operated in Parallel[1]	Eight BPK 5V74 Operated in Parallel[1]	Eight BPK 5V74 Multiplexed One at a Time[1]
Capacity	512 kilobytes	2048 kilobytes	8 megabyte	8 megabyte
Average Data Rate (kilobits/sec)	136	544	1088	136
Maximum Date Rate (kilobits/sec) (Burst)	200	800	1600	200

NOTE:
1. Multiple Bubble subsystems can be operated in parallel for maximum performance or multiplexed to conserve power.

BPK 5V74 POWER SUPPLY REQUIREMENTS

Voltage	Margin	Power Off/Power Fail Decay Rate
+12 Volt	±1%	less than 1.10 volts/msec
+5 Volt	±5%	less than 0.45 volts/msec

- Voltage sequencing — no restrictions
- Power on voltage rate of rise — no restrictions
- The power supply requirements based on recommended power fail circuitry as shown in Figure 3.
- The 12V ±1% may be supplied by:
  1. Using such power supply.
  2. Use voltage regulator with 5V ± 5% input and 12V ±1% output as used in BPK 5V75 prototype kit. Circuitry — See Figure 4.

BPK 5V74 POWER CONSUMPTION

(Includes 7114, 7234, 7244, 7250, 7264)

Standby	Typical:	0.7 W
	Maximum:	1.8 W
Active	Typical:	3.7 W
	Maximum:	6.2 W

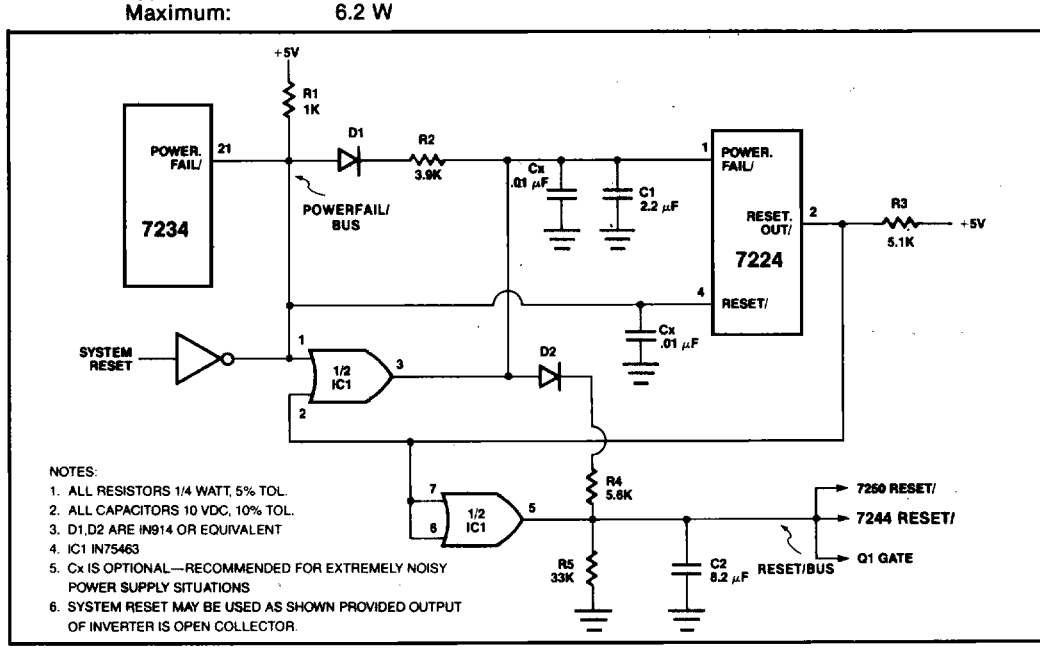


Figure 3. Power Fail Circuit

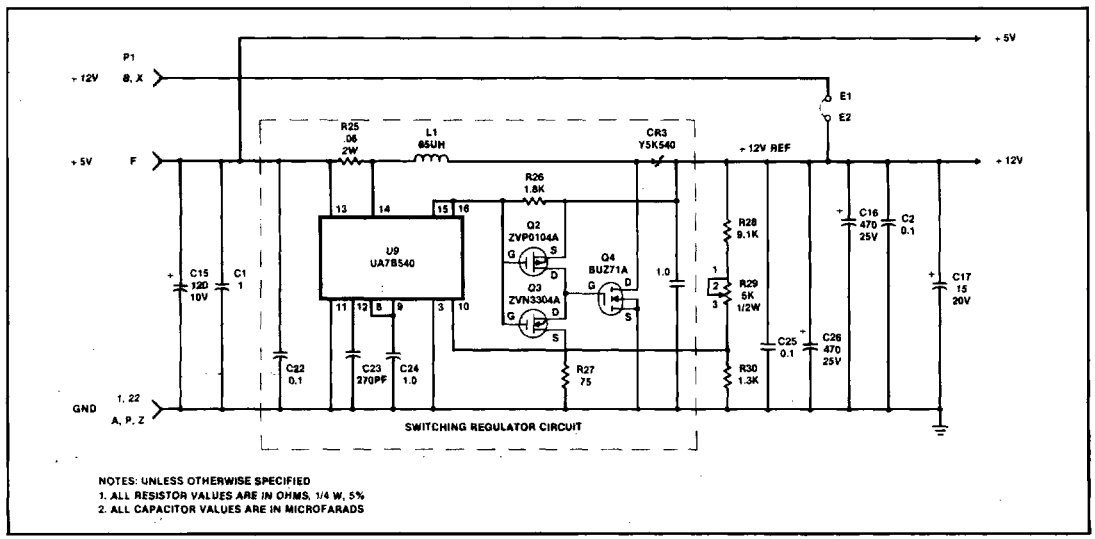


Figure 4. BPK 5V75 Voltage Regulator Circuit

PIN DESCRIPTIONS

7114

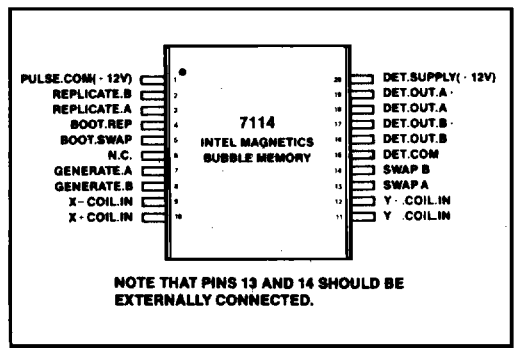


Figure 5. 7114 Pin Configuration

Table 1. 7114 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
BOOT.REP	4	I	7234 CPG	Two-level current pulse input for reading the boot loop.
BOOT.SWAP	5	I	7234 CPG	Single-level current pulse for writing data into the boot loop. This pin is normally used only in the manufacture of the MBM.
DET.COM	15	I		Ground return for the detector bridge.
DET.OUT	16 — 19	O	7244 FSA	Differential pair (A+, A− and B+, B−) outputs which have signals of several millivolts peak amplitude.
DET.SUPPLY	20	I		+12 volt supply pin.
GEN.A and GEN.B	7, 8	I	7234 CPG	Two-level current pulses for writing data onto the input track.
PULSE.COM	1	I		+12 volt supply pin.
REP.A and REP.B	3, 2	I	7234 CPG	Two-level current pulses for replicating data from storage loops to output track.
SWAP.A and SWAP.B	13, 14	I	7234 CPG	Single-level current pulse for swapping data from input track to storage loops.
X−.COIL.IN. X+COIL.IN.	9, 10	I	7264	Terminals for the X or inner coil.
Y−.COIL.IN. Y+.COIL.IN.	11, 12	I	7264	Terminals for the Y or outer coil.

7234

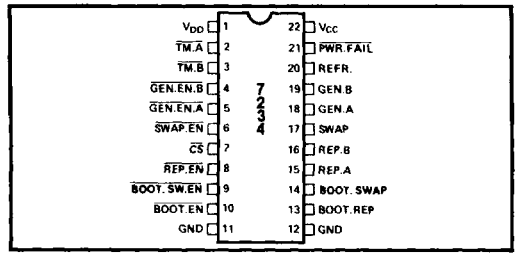


Figure 6. 7234 Pin Configuration

Table 2. 7234 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
$\overline{\text{BOOT.EN}}$	10	I	7224 BMC	An active low input enabling the BOOT.REP output current pulse.
BOOT.REP	13	O	7114 MBM	An output providing the current pulse for bootstrap loop replication in the bubble memory.
BOOT.SWAP	14	O	7114 MBM	An output providing a current pulse which may be used for writing data into the bootstrap loop.
$\overline{\text{BOOT.SW.EN}}$	9	I	7224 BMC	An active low input enabling the BOOT.SWAP output current pulse.
CS	7	I	7244 FSA	An active low input for selecting the chip. The chip powers down during deselect.
GEN.A	18	O	7114 MBM	An output providing the current pulse for writing data into the "A" quads of the bubble memory.
GEN.B	19	O	7114 MBM	An output providing the current pulse for writing data into the "B" quads of the bubble memory.
$\overline{\text{GEN.EN.A}}$	5	I	7244 FSA	An active low input enabling the GEN.A output current pulse.
$\overline{\text{GEN.EN.B}}$	4	I	7244 FSA	An active low input enabling the GEN.B output current pulse.
$\overline{\text{PWR.FAIL}}$	21	O	7224 BMC	An active low, open collector output indicating that either V_{CC} or V_{DD} is below its threshold value.
REFR.	20	I	External Resistor	The pin for the reference current generator to which an external resistance must be connected.
REP.A	15	O	7114 MBM	An output providing the current pulse for replication of data in the "A" quads of the bubble memory.
REP.B	16	O	7114 MBM	An output providing the current pulse for replication of data in the "B" quads of the bubble memory.
$\overline{\text{REP.EN}}$	8	I	7224 BMC	An active low input enabling the REP.A and REP.B outputs.
SWAP	17	O	7114 MBM	An output providing the current pulse for exchanging the data between the input track and the storage loops in the bubble memory.
$\overline{\text{SWAP.EN}}$	6	I	7224 BMC	An active low input enabling the SWAP output.
$\overline{\text{TM.A}}$	2	I	7224 BMC	An active low timing signal determining the cut pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.
$\overline{\text{TM.B}}$	3	I	7224 BMC	An active low timing signal determining the transfer pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.

7244

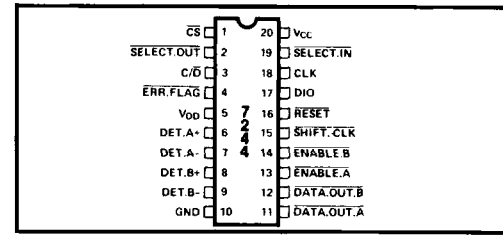


Figure 7. 7244 Pin Configuration

Table 3. 7244 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
C/$\overline{D}$	3	I	7224 BMC	Command/$\overline{\text{Data}}$ signal. This signal shall cause the FSA to enter a receive command mode when high and to interpret the serial data line as data when low. Any previously active command will be immediately terminated by C/$\overline{D}$.
CLK	18	I	Clock	Same TTL-level clock used to generate internal timing as used for 7220-1.
$\overline{CS}$	1	I	External	An active low signal used for multiplexing of FSAs. The FSA is disabled whenever $\overline{CS}$ is high (i.e., it presents a high impedance to the bus and ignores all bus activity).
$\overline{DATA.OUT.A}$, $\overline{DATA.OUT.B}$	11, 12	O	7234 CPG	Output data from the FIFO to the MBM generate circuitry. Used to write data into the bubble device (active low).
DET.A+, DET.A−, DET.B+, DET.B−	6, 7, 8, 9	I	7114 MBM	Differential signal lines from the MBM detector.
DIO	17	I/O	7224 BMC	The Serial Bus data line (a bidirectional active high signal).
$\overline{ENABLE.A}$, $\overline{ENABLE.B}$	13, 14	O	7234 CPG/7250	TTL-level outputs utilized as chip selects for other interface circuits. They shall be set and reset by the Command Decoder under instruction of the Controller (active low).
$\overline{ERR.FLG}$	4	O	7224 BMC	An error flag used to interrupt the Controller to indicate that an error condition exists. It shall be an open drain, active low signal.
$\overline{RESET}$	16	I	Power Fail Circuit	An active low signal that shall reset all flags and pointers in the FSA as well as disabling the chip as the CS signal does. The $\overline{RESET}$ pulse width must be 5 clock periods to assure the FSA is properly reset.
$\overline{SELECT.IN}$	19	I	7224 BMC	An input utilized for time-division multiplexing. An active low signal whose presence indicates that the FSA is to send or receive data from the Serial Bus during the next two clock periods.
$\overline{SELECT.OUT}$	2	O	7244 FSA	The $\overline{SELECT.IN}$ pulse delayed by two clocks. It shall be connected to the $\overline{SELECT.IN}$ pin of the next FSA. It is delayed by two clocks because the FSA is a dual-channel device. Channel A shall internally pass $\overline{SELECT.IN}$ to Channel B (delayed by one clock).
$\overline{SHIFT.CLK}$	15	I	7224 BMC	A Controller-generated clock signal that shall be used to clock data out of the bubble I/O Output Latch to the bubble module during a write operation and to cause bubble signals to be converted by the Sense Amp and clocked into the Bubble I/O Input Latch on a read.

7250

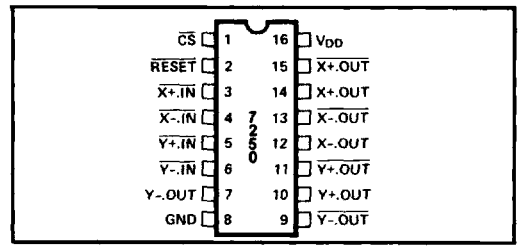


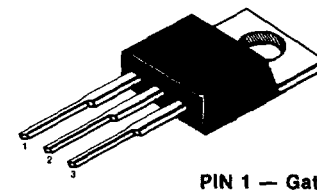
Figure 8. 7250 Pin Configuration

Table 4. 7250 Pin Description

Symbol	Pin No.	I/O	Source/Destination	Description
$\overline{CS}$	1	I	7244 FSA	Chip select. It is active low. When high chip is deselected and I_{DD} is significantly reduced.
$\overline{RESET}$	2	I	Power Fail Circuit	Active low input from RESET.OUT of MD7220-5 Controller forces 7250 outputs inactive so that bubble memory is protected in the event of power supply failure.
$\overline{X+.IN}$, $\overline{X-.IN}$	3, 4	I	7224 BMC	Active low inputs from Controller which turn on the high-current X outputs.
X−.OUT $\overline{X-.OUT}$ $\overline{X+.OUT}$ X+.OUT	12, 13, 14, 15	O	7264	High-current outputs and their complements for driving the gates of the 7264 transistors which in turn drive the X coils of the bubble memory.
$\overline{Y+.IN}$, $\overline{Y-.IN}$	5, 6	I	7224 BMC	Active low inputs from Controller which turn on the high-current Y outputs.
Y−OUT $\overline{Y-.OUT}$ $\overline{Y+.OUT}$ Y+.OUT	7,9,10,11	O	7264	High-current outputs and their complements for driving the gates of the 7264 quad transistors which in turn drive the Y coils of the bubble memory.

7264

Four matched pair of N- and P-channel transistors. In industry standard TO-220 Discrete packaging.



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

Symbol	Pin No.	I/O	Source/Destination	Description
N-Channel				
G	1	I	7250	Gate Drive Signal
D	2	O	7114	Coil Drive Current
S	3	I	Ground	—
P-Channel				
G	1	I	7250	Gate Drive Signal
D	2	O	7114	Coil Drive Current
S	3	I	Ground	—

ABSOLUTE MAXIMUM RATINGS*

7114

Operating Temperature ..... 10°C to 55°C Case
Relative Humidity 95%
Shelf Storage Temperature (Data Integrity Not Guaranteed) ..... −55°C to +125°C
Voltage Applied to DET.SUPPLY ..... 14 Volts
Voltage Applied to PULSE. COM ..... 14 Volts
Continuous Current between DET.COM and Detector Outputs ..... 20 mA
Coil Current ..... 0.5A D.C.
External Magnetic Field for Non-Volatile Storage ..... 20 Oersteds
Non-Operating Handling Shock (without socket) 200G
Operating Vibration (2 Hz to 2 kHz with socket) 20G

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

SUPPORT I.C.'S

	7234	7244	7250	7264
Temperature Under Bias	−40 to 100°C	−10 to +85°C	−40 to 100°C	−40 to 100°C
Storage Temperature	−65 to +150°C	−65 to +150°C	−65 to +150°C	−55 to +150°C
Voltage Input	−0.5 to +7V		−0.5 to V_{DD} +0.5	
V_{CC}	−0.5 to +7V	−0.5 to +7V		
V_{DD}	−0.5 to +12.6V	−0.5 to +14V		
Gate Voltage				15V
Output Current			250mA	
Power Dissipation 80°C	1W			1.05W
Power Dissipation 25°C		1W		2W
Continuous Drain Current				2A
Peak Drain Current				3A

D.C. CHARACTERISTICS

The BPK 5V74 is designed as a true subsystem. All D.C. characteristics that describes the interfacing to the subsystem is included in this section.

7234 (T_A 0°C to +70°C; V_{CC} = 5.0V ±5%, ±5% V_{DD} = 12V ±5%; unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{IL}	Input Low Current			−0.4	mA	V_{IL} = 0.4V, V_{CC} = 5.25V
I_{IH}	Input High Current			20	μA	V_{IH} = V_{CC} = 5.25V
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_C	Input Clamp Voltage			−1.5	V	I = −18 mA, V_{CC} = 4.75V
I_{CEX1}	Output Leakage Current (All Outputs except PWR.FAIL)			1.0	mA	V_{CC} = 5.25V, V_{DD} = 12.6V
I_{CEX2}	$\overline{\text{PWR.FAIL}}$ Output Leakage Current			40	μA	V_{OH} = V_{CC} = 5.25V
V_{OL}	$\overline{\text{PWR.FAIL}}$ Output Low Voltage			0.4	V	I_{OL} = 4 mA, V_{CC} = 4.75V
I_{CC1}	Current from V_{CC}—Selected		30	45	mA	CS = V_{IL}, V_{CC} = 5.25V
I_{DD1}	Current from V_{DD}—Selected		20	35	mA	CS = V_{IL}, V_{CC} = 5.25V
I_{DD2}	Current from V_{DD}—Power Down		12	19	mA	CS = V_{IH}, V_{DD} = 12.6V

7244 (T_A = 0°C to 70°C; V_{CC} = 5.0V +5%, −10%: V_{DD} = 12V ±5%)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage (All Outputs Except $\overline{\text{SELECT.OUT}}$)			0.45	V	I_{OL} = 3.2mA
V_{OLSO}	Output Low Voltage ($\overline{\text{SELECT.OUT}}$)			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage (All Outputs Except $\overline{\text{SELECT.OUT}}$)	2.4			V	I_{OH} = 400 μA
V_{OHSO}	Output High Voltage ($\overline{\text{SELECT.OUT}}$)	2.4			V	I_{OH} = 200 μA
V_{THR}	Detector Threshold		6.8		mV	V_{DD} = 12.0V
$\lvert I_{IN} \rvert$	Input Leakage Current			10	μA	$0 \leq V_{IN} \leq V_{CC}$
$\lvert I_{OFL} \rvert$	Output Float Leakage			10	μA	$0.45 \leq V_{OUT} \leq V_{CC}$
I_{CC}	Power Supply Current from V_{CC}			120	mA	
I_{DD}	Power Supply Current from V_{DD}			30	mA	

7250 (T_A = 0° to 70°C; V_{DD} = 12V +5%, −10%; unless otherwise specified)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
$\|I_{IN}\|$	Input Current			5	μA	V_I = 0.8V
V_{IL}	Low-Level Input Voltage			0.8	V	
V_{IH}	High-Level Input Voltage	2.2			V	
I_{DD0}	Supply Current			4.5	mA	Chip Deselected: $\overline{CS}$ = V_{IH}, V_{DD} = 12.6V
I_{DD1}	Supply Current			75	mA	f = 100 kHz, V_{DD} = 12.6V, Outputs Unloaded