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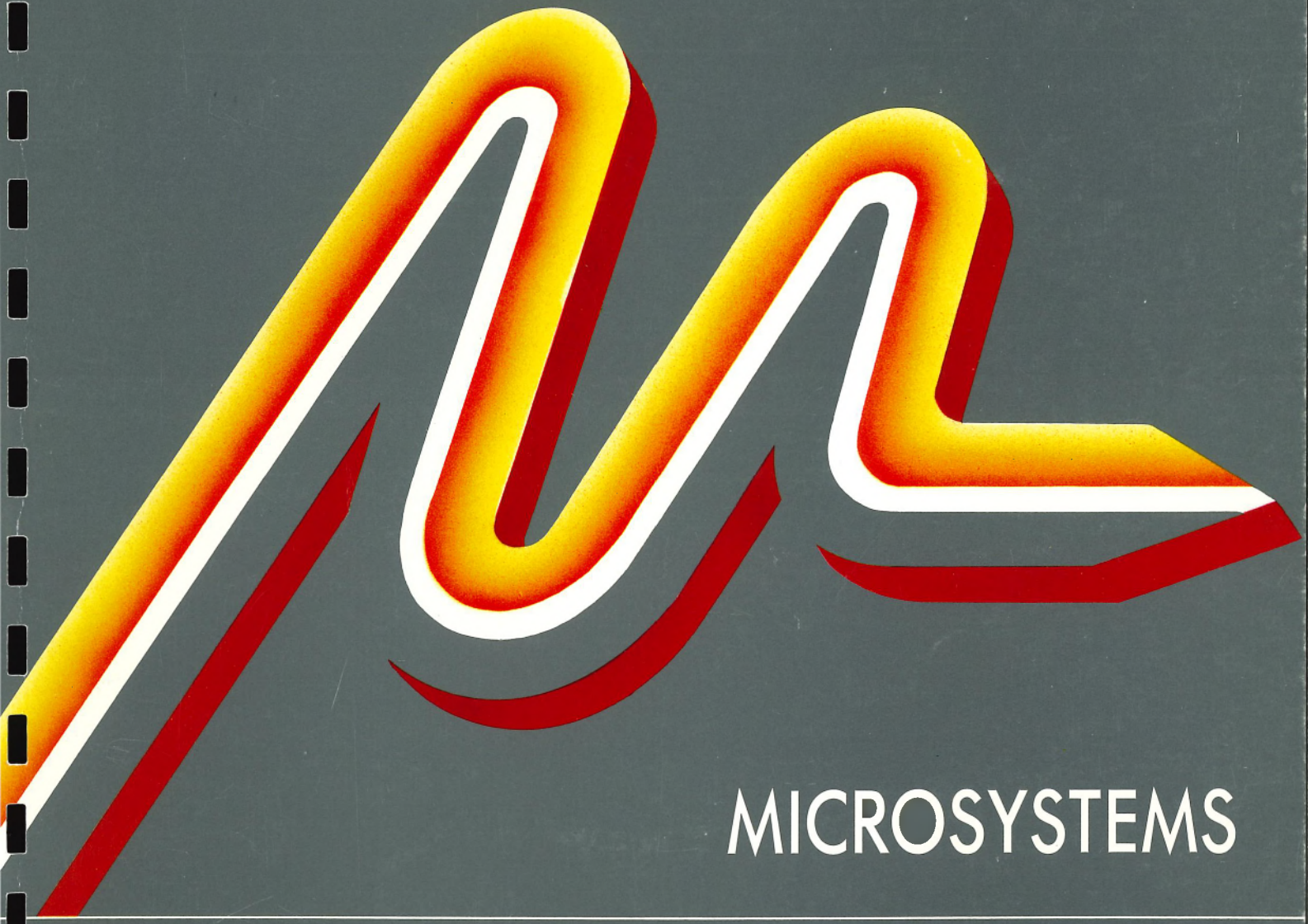


MICROSYSTEMS

[redacted]

THOMSON SEMICONDUCTEURS

TSVME 204

RAM/EPROM memory board

USER'S MANUAL

TSVME 204
RAM/EPROM
memory board
A001 - 02

CONTENTS

1 - GENERAL INFORMATION

The TSVME204 board is a VME bus compatible double eurocard (revision C), a memory module belonging to the standard board family from VMEbus Thomson semiconductors.

The TSVME204 board comprises 24 component sockets for a 28-pin standard Jedec.

It has been designed to accept all types of memory (RAM, EPROM, EEprom) currently available on the market or which are being developed.
A battery enables a data back-up to be performed if RAM CMOS memories are used.

The board is divided into 3 blocks of 8 Jedec sockets, with totally independent base addresses, types of unit and access mode.

2 - LAYOUT

The TSVME204 board is divided into 3 blocks of 8 x 28-pin Jedec sockets, each block being independent and separately configurable:

- jumper selectable access time
- memory type: RAM, REPROM, EEPROM
- unit capacity : 8K x 8, 16K x 8, 32K x 8, 64K x 8
- selectable access mode:

* read and write or read only (REPROM)
* supervisor mode and/or user
* data mode and/or program

- base address selectable over the entire VME bus 16 Mbyte area (standard addressing).

The board chains the arbitration signals of the VME bus as well as the acknowledge interrupt signals, which means that board location does not affect system operation.

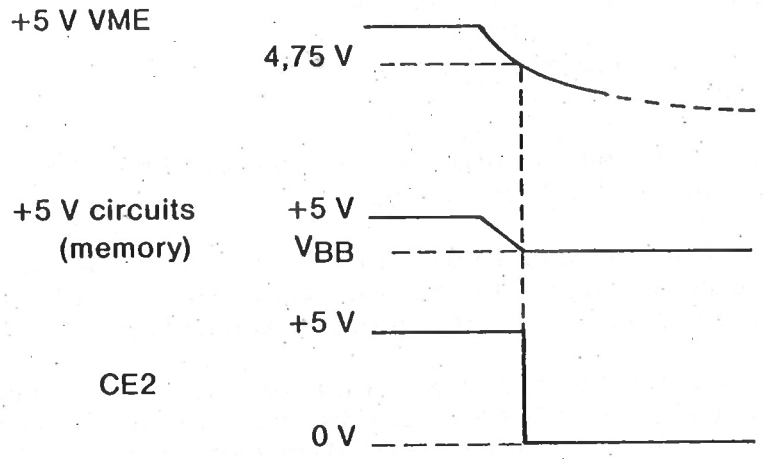
An on-board battery allows one block to be saved in the event of mains failure if CMOS units are used. Three light-emitting diodes enable the user to display access to the different blocks on the front panel.

2.1 - USE OF A CMOS MEMORY BLOCK BATTERY BACK UP

It is possible to save a RAM CMOS memory block by means of the local battery if the VME bus +5V power supply fails.

The "Power fail" detection module enables the memory block power supply to be switched over to the 5V back-up if the power supply drops. Furthermore the module deactivates the CE2 signal in order to place the circuits in the low power consumption "Standby" position and to forbid access to the block.

Power fail module operating principle :



VBB signal: battery voltage

Detection of a drop in voltage takes place at 4.75V, the VME norm sets the 5V line at +0.25V, -0.125V.

CAUTION: The "Power Fail" module allows one block only to be saved. Therefore, it is imperative to select one block only in back-up mode.

2.2 - JEDEC FORMAT

All the 28-pin sockets on the board are designed to receive, for each 8 socket block, memory circuits with a Jedec compatible pin layout.

The Jedec norm sets a standard, with a number of pins assigned specifically to circuits according to their types or capacities:

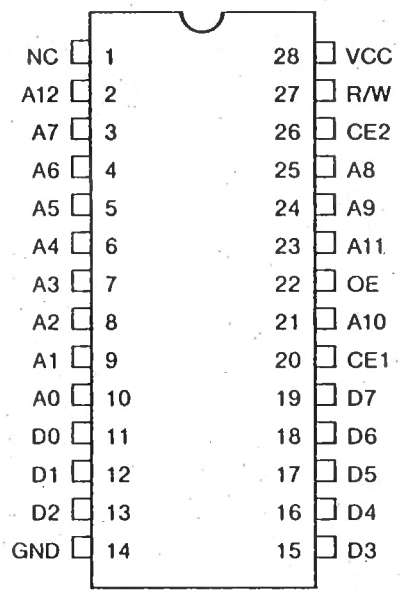
Pins	3 to 10	Ao to A7
	11 to 13 and 15 to 19	Do - D7
	20	CE
	22	OE
	21,23 to 25	A8 - A11

Table of the pins specific to each unit

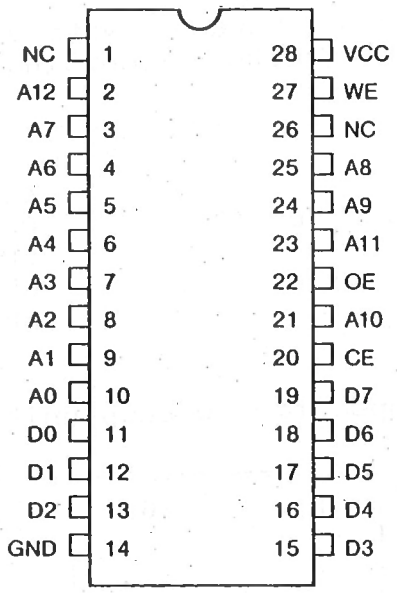
PINS / UNITS	1	26	27
RAM 8K x 8	NC	CE2	WE
EEPROM 8K x 8	NC	NC	WE
REPROM 8K x 8	VPP	NC	PGM
16K x 8	VPP	A13	PGM
32K x 8	VPP	A13	A14
64K x 8	A15	A13	A14

Pin layout of the different circuits possible on the TSVME204 board.

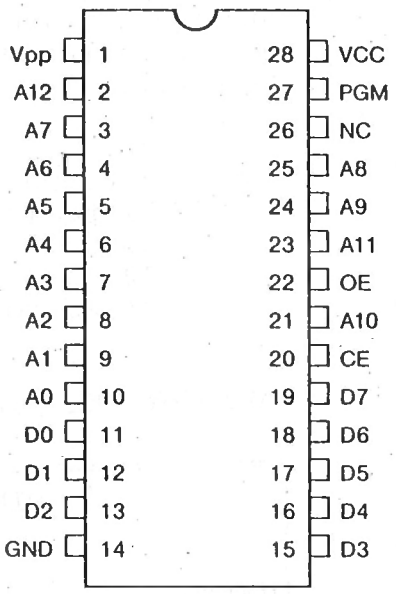
STATIC RAM
8K x 8



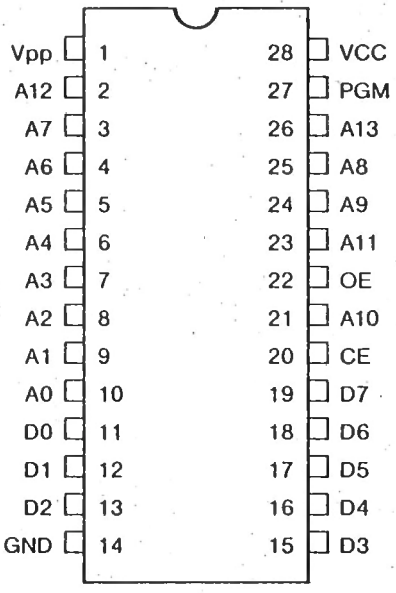
EEPROM
8K x 8



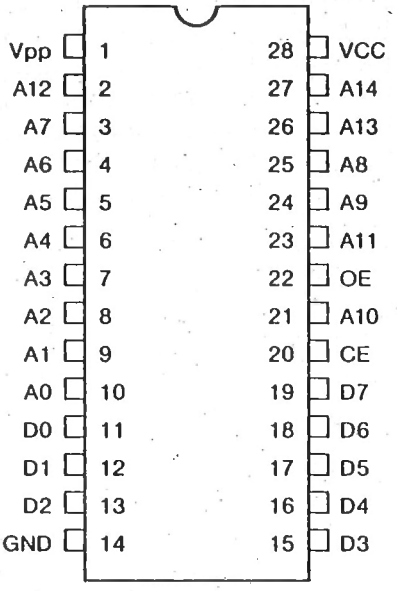
ROM/EPROM
8K x 8



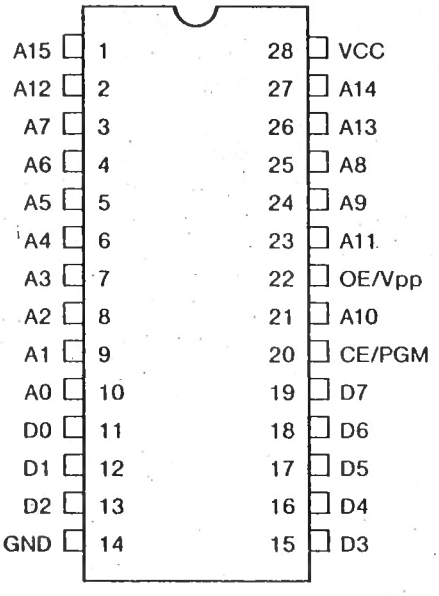
ROM/EPROM
16K x 8



ROM/EPROM
32K x 8



ROM/EPROM
64K x 8



2.3 - VME BUS INTERFACE

The TSVME204 board VME bus interface is slave type. It corresponds to revision C of the VME specifications. The signals specific to bus arbitration and interrupt management are not managed by the board.

Only the "daisy chain" signals (BGxIN, BGxOUT and IACKIN - IACKOUT) are chained so that board location in the backplane does not affect system operation.

The interface comprises an IACK detection signal in order to differentiate between memory access and acknowledge interrupt access.

The interface comprises address modifier management in order to distinguish the different addressing modes: short, standard, extended. Only standard addressing enables the board to be accessed. The supervisor, user, data and program access modes are jumper selected.

3 - TECHNICAL SPECIFICATIONS

3.1 - TSVME204 BOARD TECHNICAL SPECIFICATIONS

Architecture	3 independent blocks
Capacity	24 x 28-pin Jedec sockets
Back-up	by means of a local battery or the +5V STANDBY line of the VME bus
Data format	8 bit bytes 16 bit words
Access cycles	read, write, "Read modify write"
Power supply	+5V dc +5%; ,2.5%
Consumption on memory	I max 1.5 A
Operating temperature Storage temperature	5 to 55 degrees C -40 to +70 degrees C
Humidity	0 to 95% without condensation
Front panel board dimension	233.5mm 160mm Standard (GME x GTE= 262 x 20mm)

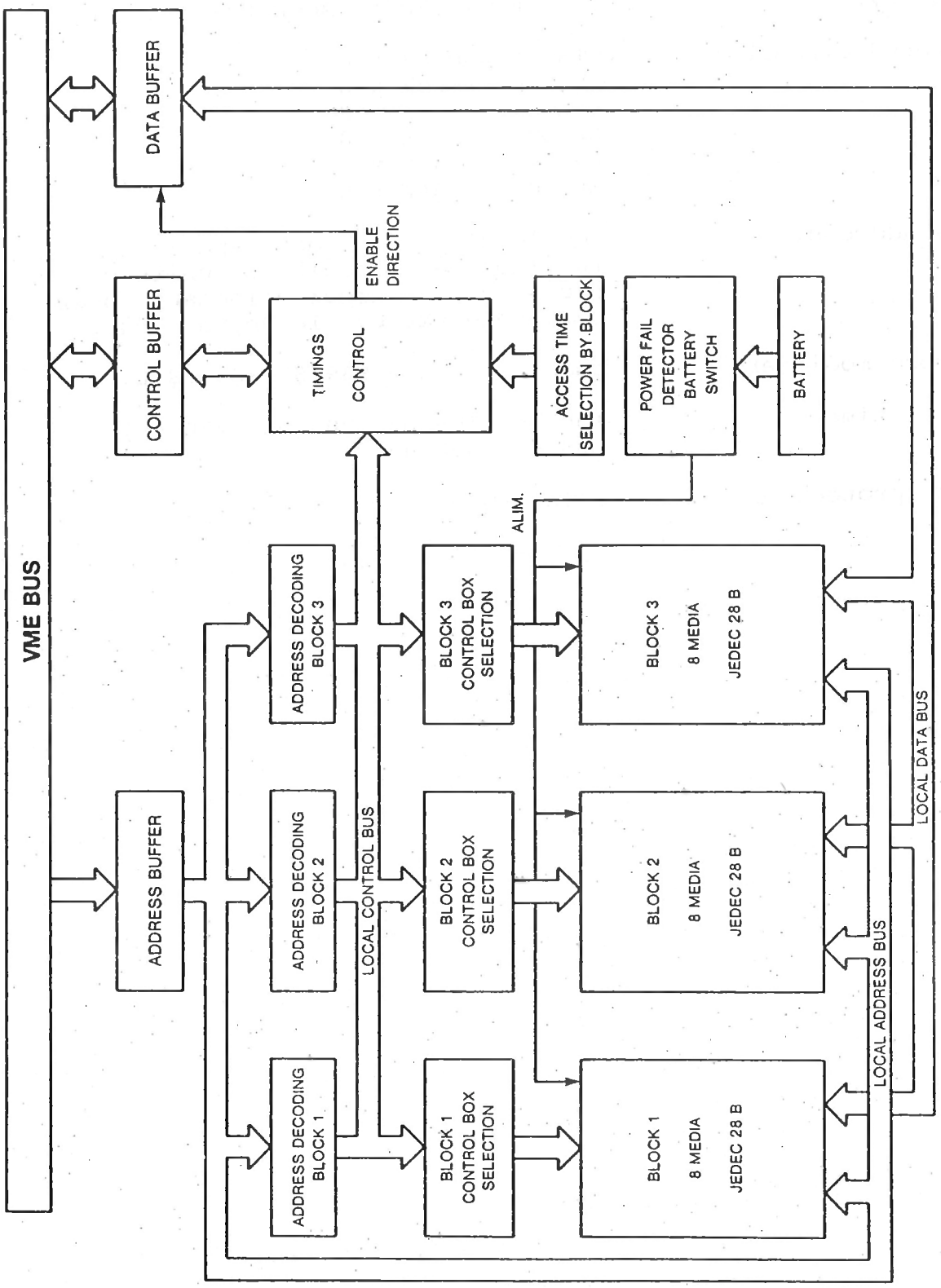
3 diodes located on the front panel indicate block access to the user.

NOTE : To ascertain board consumption when it is equipped, add the above consumption to the amount consumed by the on-board memories.

3.2 - TSVME204 BOARD TECHNICAL SPECIFICATIONS PER BLOCK

Capacity:	8 x 28-pin Jedec sockets
Accepted circuits:	STATIC RAM 8K x 8 EEPROM 8K x 8 EPROM 8K x 8 EPROM 16K x 8 EPROM 32K x 8 EPROM 64K x 8
Base address:	Modulo of total block capacity (8 times the capacity of units on the block). Jumper-selectable over the whole VME bus 16 Mbyte range.
Address modifiers:	codes accepted $39-$3A-$3D-$3E.
Access time:	100 ns, 150 ns, 200 ns, 250 ns, 350 ns, 500 ns
Write protection:	selectable

4 - BLOCK DIAGRAM



5 - SELECTORS

Table of the TSVME204 board selectors

Selectors	Function	Block
S1	addressing capacity	3
S2	addressing capacity	2
S3	addressing capacity	1
S4	address modifiers	3
S5	address modifiers	2
S6	address modifiers	1
S7	base address	3
S8	base address	2
S9	base address	1
S10	memory configuration	3
S11	memory configuration	2
S12	memory configuration	1
S13	access time	3
S14	access time	2
S15	access time	1
S16	battery/VME standby	1.2 and 3
S17	power supply	3
S18	power supply	2
S19	power supply	1
S20	write protection	1
S21	write protection	3
S22	write protection	2

6 - LOCATION PER BLOCK

6.1 - BOARD LOCATION PER BLOCK

Block 1

Associated light-emitting diode: Led 1

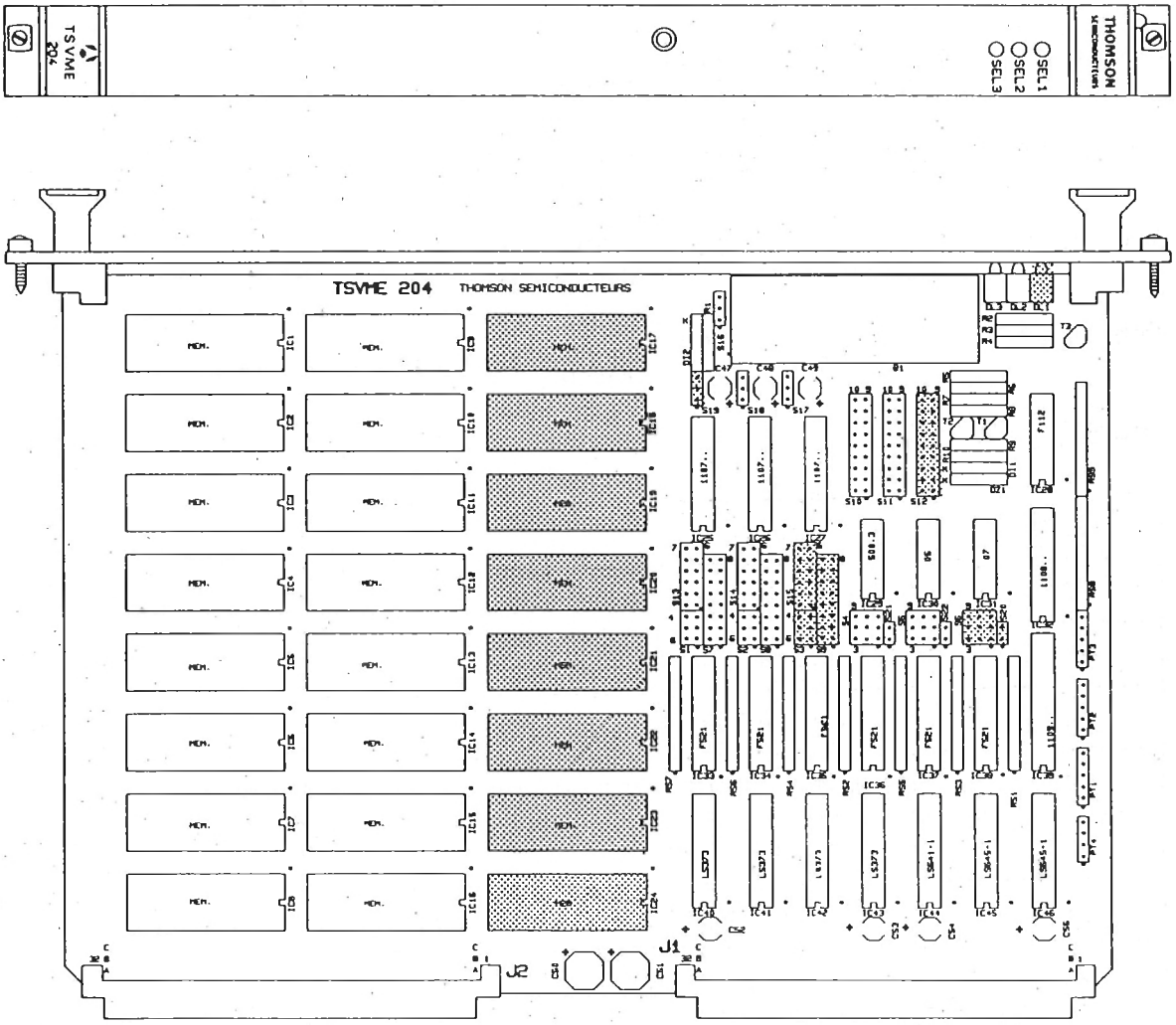
Block 1 comprises 8 sockets located from IC17 to IC24.

1st memory pair	IC24 ODD
	IC23 EVEN
2nd pair	IC22 ODD
	IC21 EVEN
3rd pair	IC20 ODD
	IC19 EVEN
4th pair	IC18 ODD
	IC17 EVEN

Associated selectors:

Selectors	Functions
S3	addressing capacity
S6	address modifiers
S9	base address
S12	memory configuration
S15	access time
S19	power supply
S20	write protection

Location of block 1 sockets and selectors



6.2 - BOARD LOCATION PER BLOCK

Block 2

Asociated light-emitting diode: Led 2

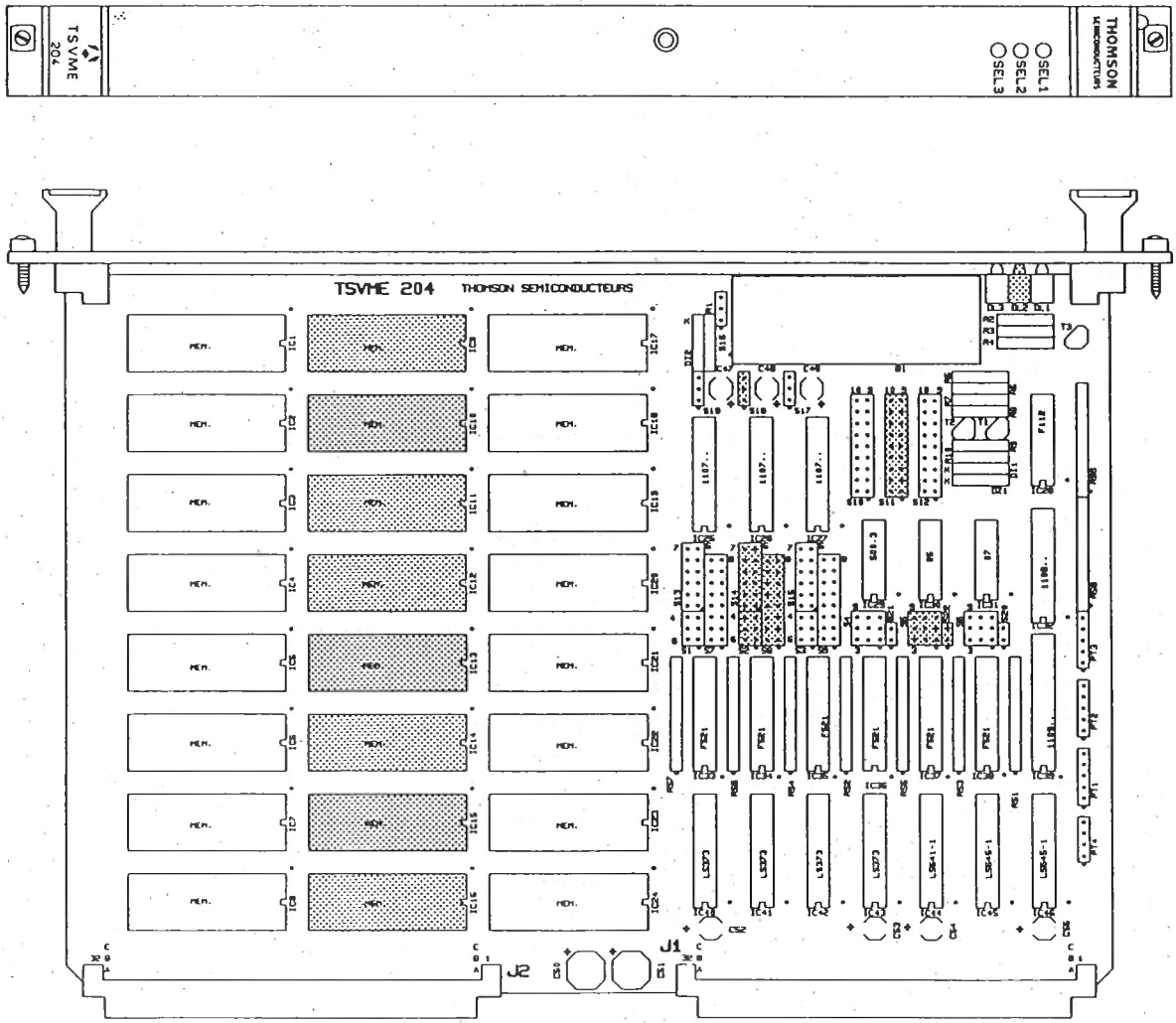
Block 2 comprises 8 sockets located from IC9 to IC16.

1st memory pair	IC16 ODD IC15 EVEN
2nd pair	IC14 ODD IC13 EVEN
3rd pair	IC12 ODD IC11 EVEN
4th pair	IC10 ODD IC 9 EVEN

Associated selectors:

Selectors	Functions
S2	addressing capacity
S5	address modifiers
S8	base address
S11	memory configuration
S14	access time
S18	power supply
S22	write protection

Location of block 2 sockets and selectors



6.3 BOARD LOCATION PER BLOCK

BLOCK 3

Associated light-emitting diode: Led 3

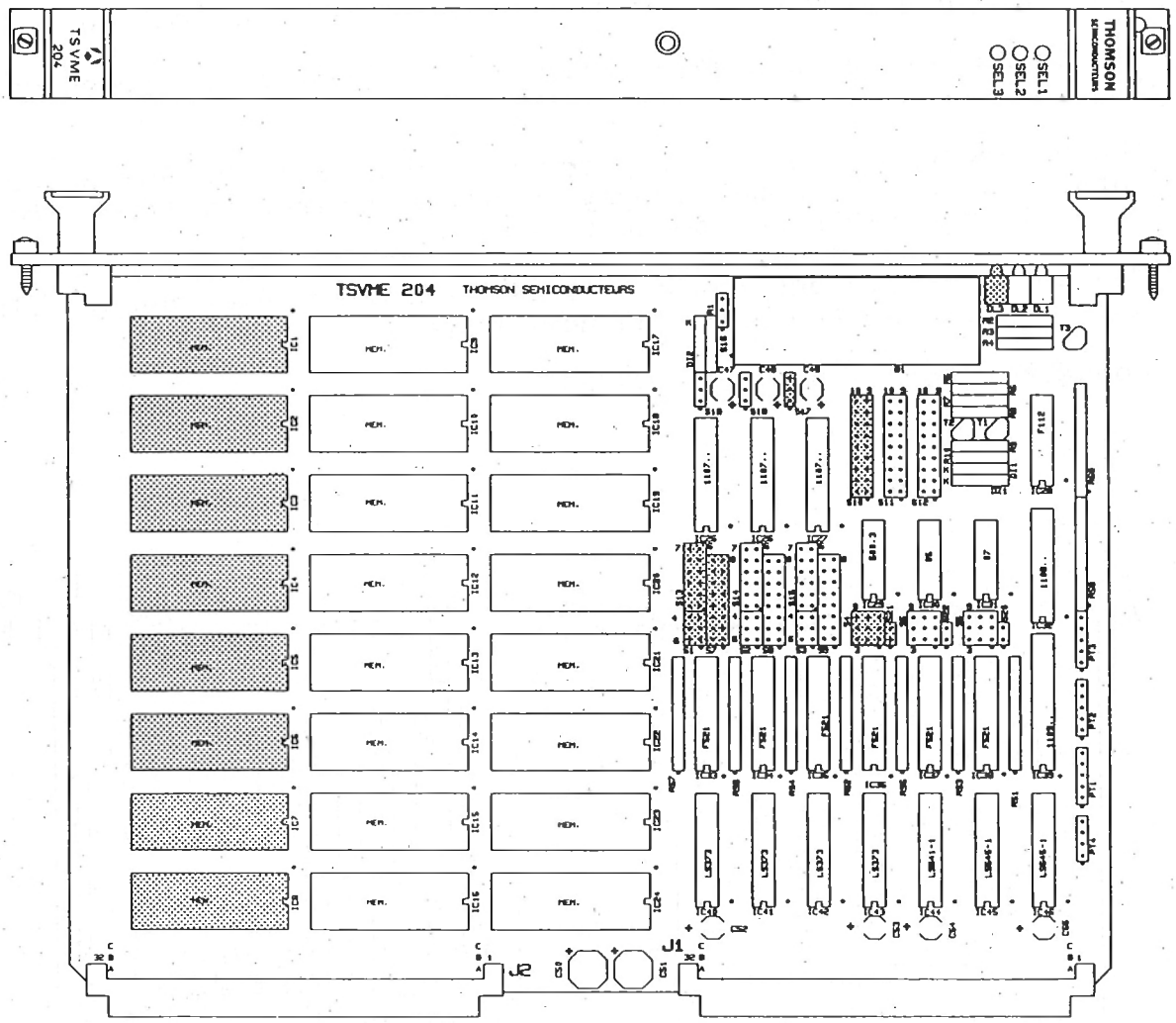
Block 3 comprises 8 sockets located from IC1 to IC8.

1st memory pair	IC8 ODD
	IC7 EVEN
2nd pair	IC6 ODD
	IC5 EVEN
3rd pair	IC4 ODD
	IC3 EVEN
4th pair	IC2 ODD
	IC1 EVEN

Associated selectors:

Selectors	Functions
S1	addressing capacity
S4	address modifiers
S7	base address
S10	memory configuration
S13	access time
S17	power supply
S21	write protection

Location of block 3 sockets and selectors



7 - CONNECTORS

VME bus interface

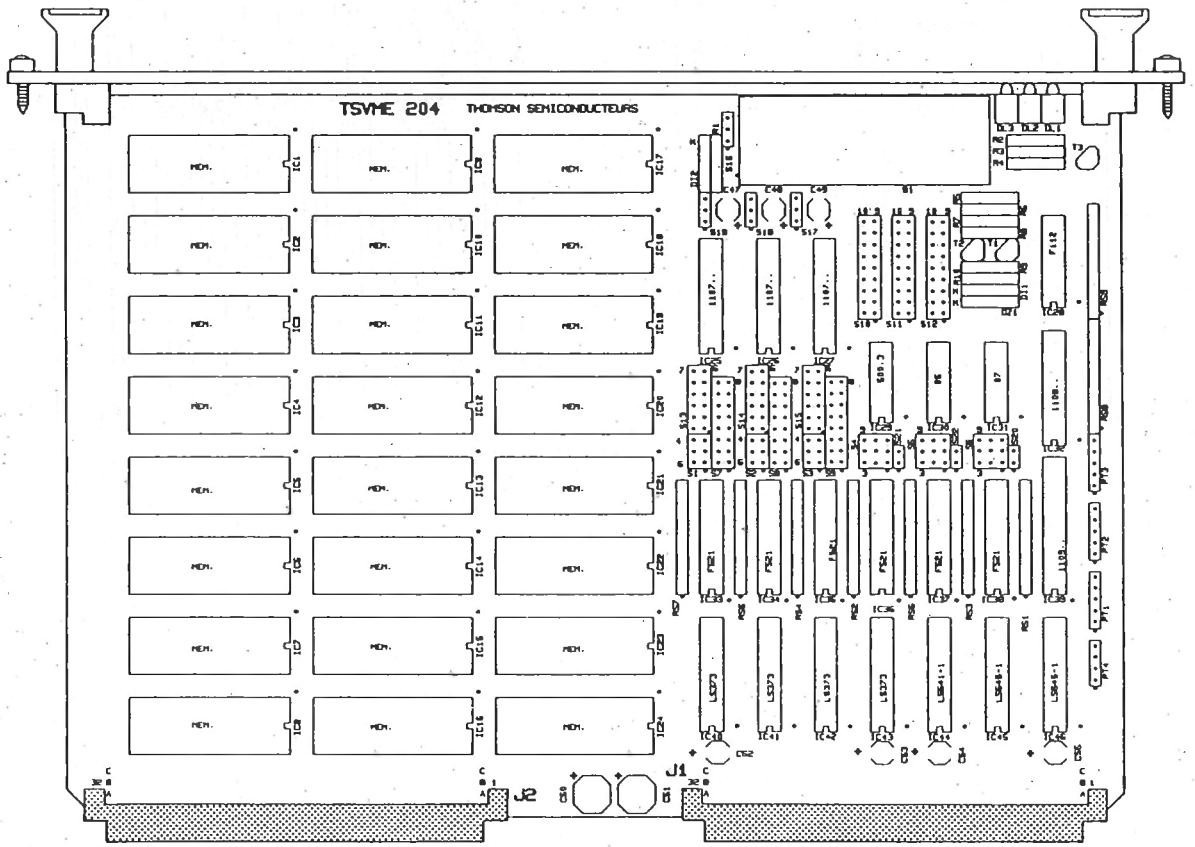
Description of the connectors associated with the VME bus

The connectors J1 and J2 are two 96-pin right angled connectors type DIN 41612C.

The connector J1 ensures the connection of all the VME control, data, address and power supply signals required by the board as shown in the table on the next page.

The connector J2 ensures only the additional power supply links as shown in the table on the next page.

Connector location on the board.



VME interface

The board uses the connector P1 and P2 of the VME bus. Signal assignment is described in the following table. The connector P2 of the VME bus is used only for the power supply pins.

A detailed description of the VME bus is given in the document "VME BUS SPECIFICATION MANUAL".

NB: A signal's name followed by * means that it is active at low logic level (0). Example: WRITE*. This code is used throughout the document.

TABLE OF SIGNALS USED - P1 -

Pin	Signal	Pin	Signal	Pin	Signal
A1	D0	B1	NU	C1	D8
A2	D1	B2	NU	C2	D9
A3	D2	B3	NU	C3	D10
A4	D3	B4	(1)BG0IN*	C4	D11
A5	D4	B5	(1)BG0OUT*	C5	D12
A6	D5	B6	(1)BG1IN*	C6	D13
A7	D6	B7	(1)BG1OUT*	C7	D14
A8	D7	B8	(1)BG2IN*	C8	D15
A9	GND	B9	(1)BG2OUT*	C9	GND
A10	SYSCLK	B10	(1)BG3IN*	C10	NU
A11	GND	B11	(1)BG3OUT*	C11	NU
A12	DS1*	B12	NU	C12	SYS/RESET*
A13	DS0*	B13	NU	C13	NU
A14	WRITE*	B14	NU	C14	AM5
A15	GND	B15	NU	C15	A23
A16	DTACK*	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS*	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK*	B20	GND	C20	A18
A21	(1)IACKIN*	B21	NU	C21	A17
A22	(1)IACKOUT*	B22	NU	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	NU	C24	A14
A25	A6	B25	NU	C25	A13
A26	A5	B26	NU	C26	A12
A27	A4	B27	NU	C27	A11
A28	A3	B28	NU	C28	A10
A29	A2	B29	NU	C29	A9
A30	A1	B30	NU	C30	A8
A31	NU	B31	+5V STDBY	C31	NU
A32	+5V	B32	+5V	C32	+5V

(1) Ensures daisy chaining only.

NB : A signal's name followed by * means that it is active at low logic level (0). E.g. : WRITE* This code is used throughout the document.

Tables of signals used - P2 -

SOCKET NUMBER	MNEMONIC SIGNAL	MNEMONIC SIGNAL	MNEMONIC SIGNAL
1		+5 Volts	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 Volts	
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31		GND	
32		+5 Volts	

8 - SELECTORS

SELECTOR CONFIGURATION PER FUNCTION

8.1 - Addressing capacity

Jumpers S1 - S2 - S3: addressing capacity.

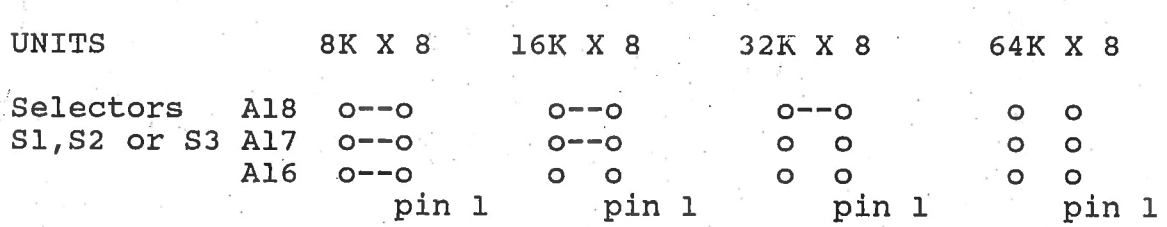
For each block, base addressing depends on the capacity of the units installed. The base address should be a multiple of the total block capacity: i.e. 8 times the capacity of the unit located on the block.

Example: for use of the 16 Kbyte memory, the base address will be modulo 128K, i.e. a multiple of $ 20000. The selectors S1, S2 and S3 may or may not permit the address lines A16, A17 and A18 to be registered in address decoding:

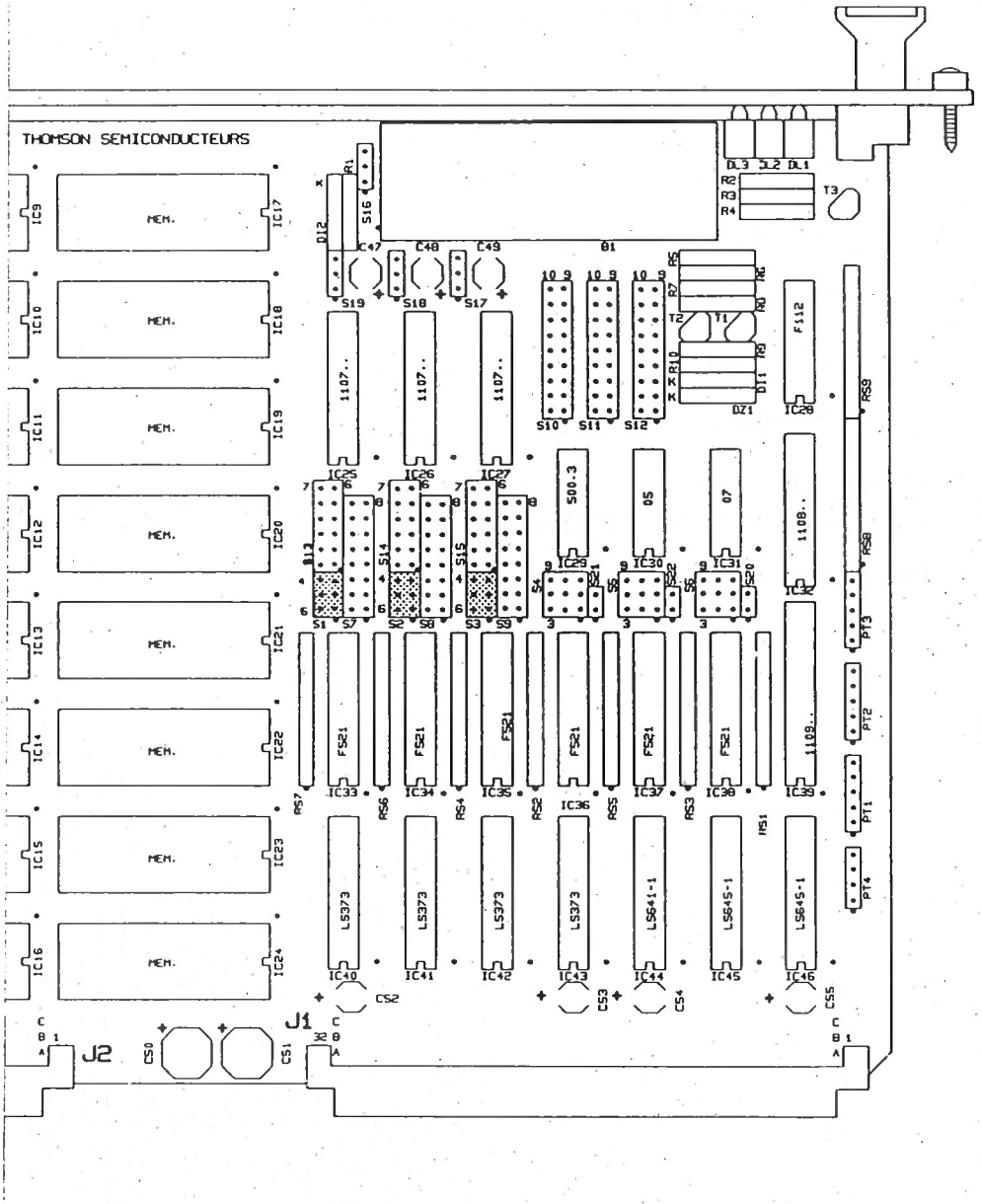
- jumper present: assigned address line registered

- jumper absent: address line unknown.

Position of the jumpers S1, S2 or S3 according to the line of units used:



Location of the selectors S1, S2 and S3 on the TSVME204 board :



8.2 ADDRESS MODIFIER DECODING SELECTORS

The decoding function of the address modifiers allows selection - in standard mode - of the board access modes.

VME bus codes: $39-$3A-$3D-$3E

It is possible to use jumpers to select access in the following modes :

either supervisor

or user

or supervisor/user

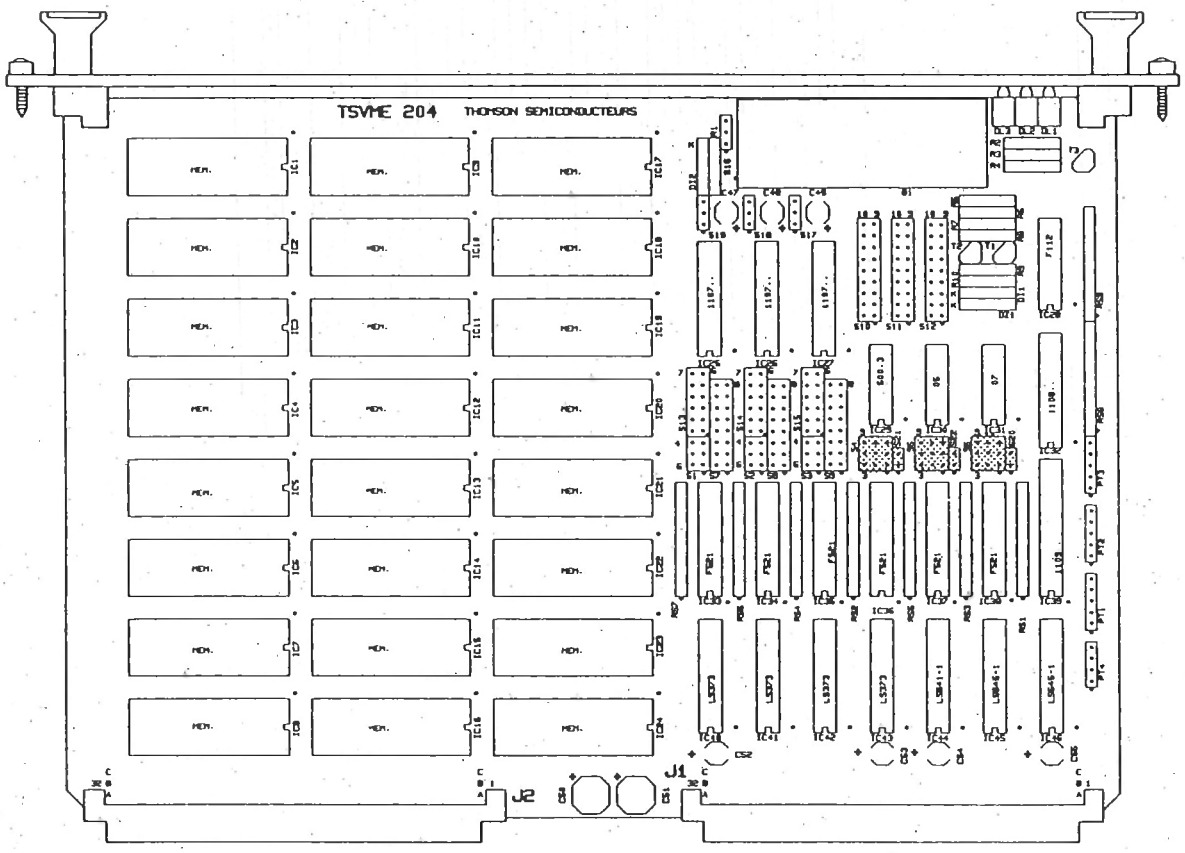
and or data

or program

or data/program.

This function is performed by the jumpers S4, S5 or S6 (according to the block desired).

Selector location on the board:



Jumper position according to the type of access desired

access	supervisor only	user only	supervisor or user
data only	o o o o o--o o o o pin 1	o o o o o--o o o--o pin 1	o o o o o--o o--o o pin 1
program only	o o--o o o o o o o pin 1	o o--o o o o o o--o pin 1	o o--o o o o o--o o pin 1
data or program	o--o o o--o o o o o pin 1	o--o o o--o o o o--o pin 1	o--o o o--o o o--o o pin 1

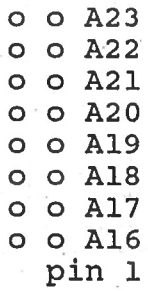
8.3 - SELECTION OF THE BOARD BASE ADDRESS PER BLOCK

For each block, the base address is selectable over the whole VME bus 16 Mbyte range.

The base address is defined by jumpers, on the selectors S7, S8 or S9 according to the block concerned.

The base address should be a multiple integer of the total block capacity (which depends on the capacity of the units located on the block.)

Selector format: S7, S8 or S9



Jumper present: board selection for the address bit corresponding to status 0

Jumper absent: board selection for the address bit corresponding to status 1

Notes:

- Jumper A16 should be absent when 16K x 8 units are used.
- Jumpers A16 and A17 should be absent when 32K x 8 units are used.
- Jumpers A16, A17 and A18 should be absent when 64K x 8 units are used

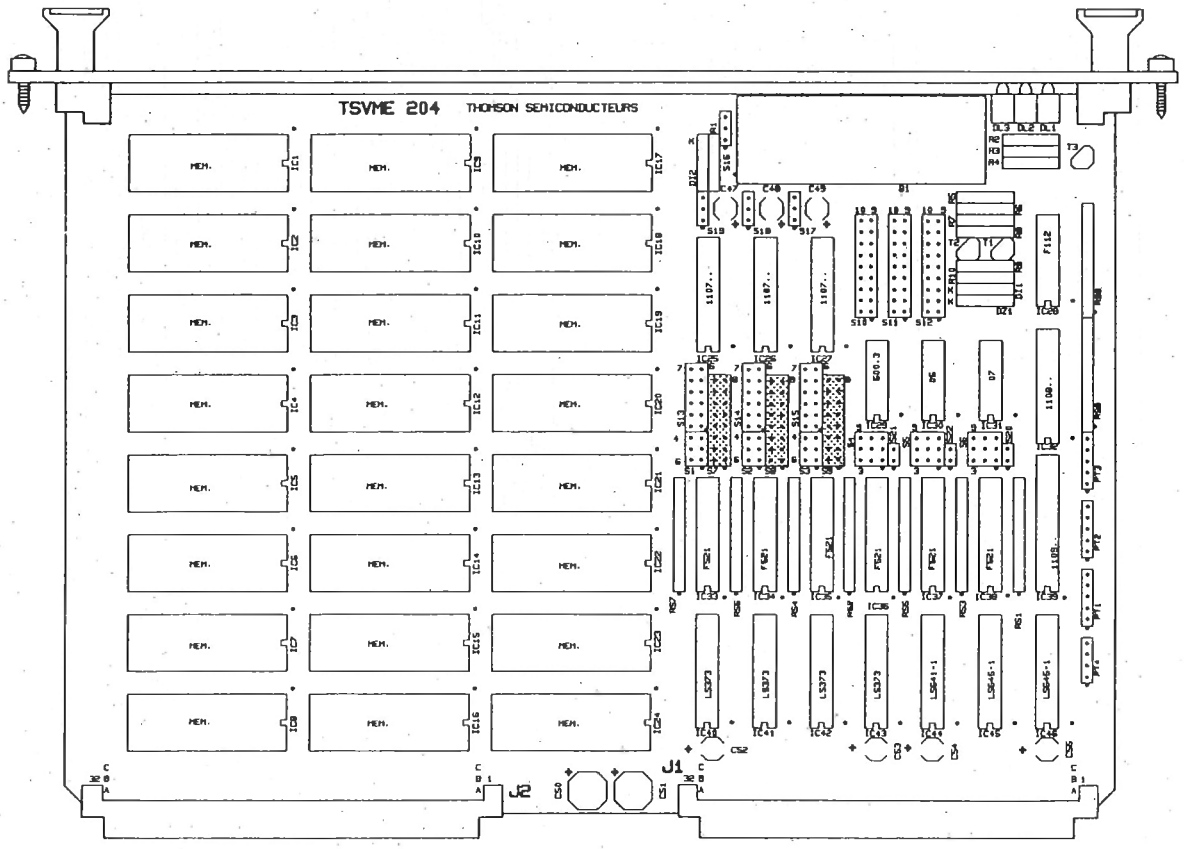
Example of base address configuration for 8K x 8 units

```
                    o--o A23
base address = $40000 o--o
                    o--o
                    o--o
                    o--o
                    o  o
                    o--o
                    o--o A16
                       pin 1
```

base address = $40000 for 32K x 8 units

```
                    o--o A23
                    o--o
                    o--o
                    o--o
                    o--o
                    o  o
                    o  o
                    o  o A16
                       pin 1
```

Location of the selectors S7, S8 and S9 on the board

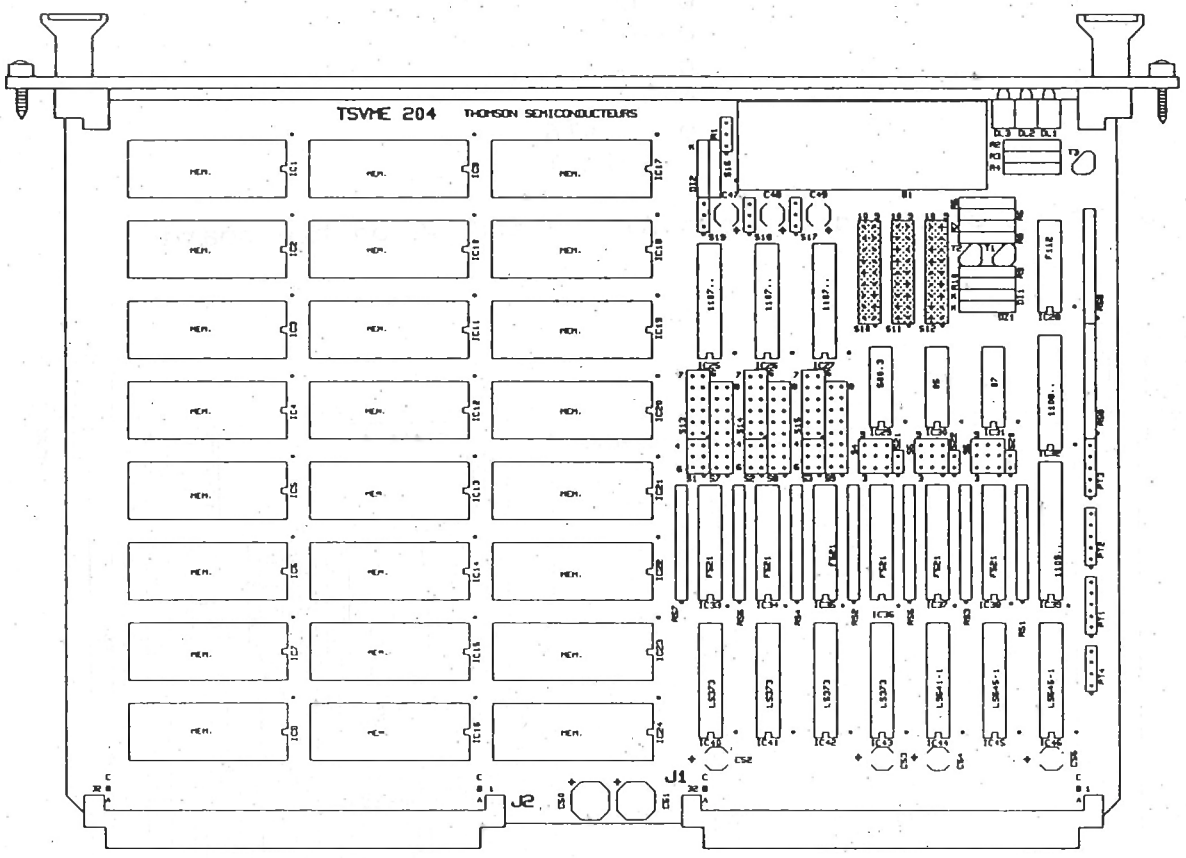


8.4 - CONFIGURATION OF MEMORY CIRCUIT SOCKETS PER BLOCK

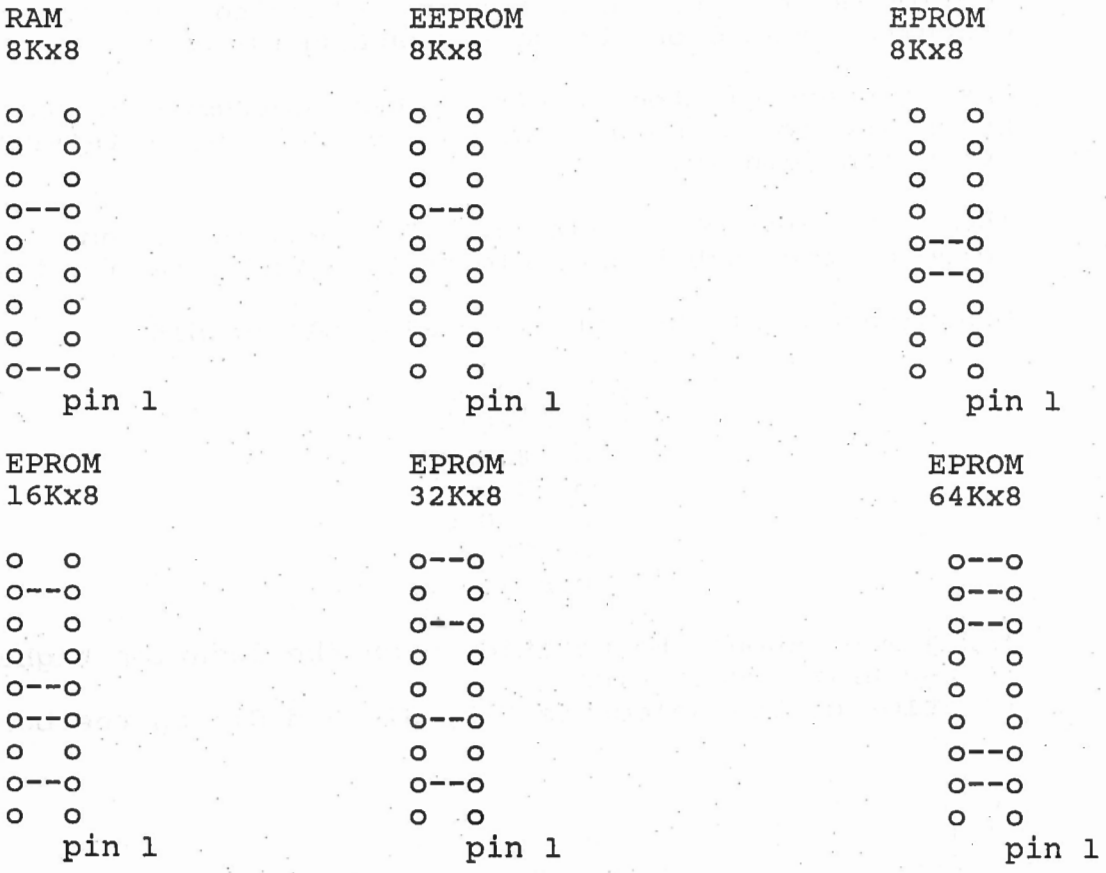
Each block may be configured by jumper for different memory types.

The selectors S10, S11, S12 perform this function for blocks 3, 2, and 1 respectively. Furthermore these selectors tell the unit selection module which addresses are to be registered in order to decode each circuit.

Selector location on the board.



Jumper position on the selectors according to the type and capacity of units located on the sockets:



8.5 - ACCESS TIME SELECTION

Each block possesses its access time selector which should be configured by just one jumper selecting the access time of circuits located on the corresponding block.

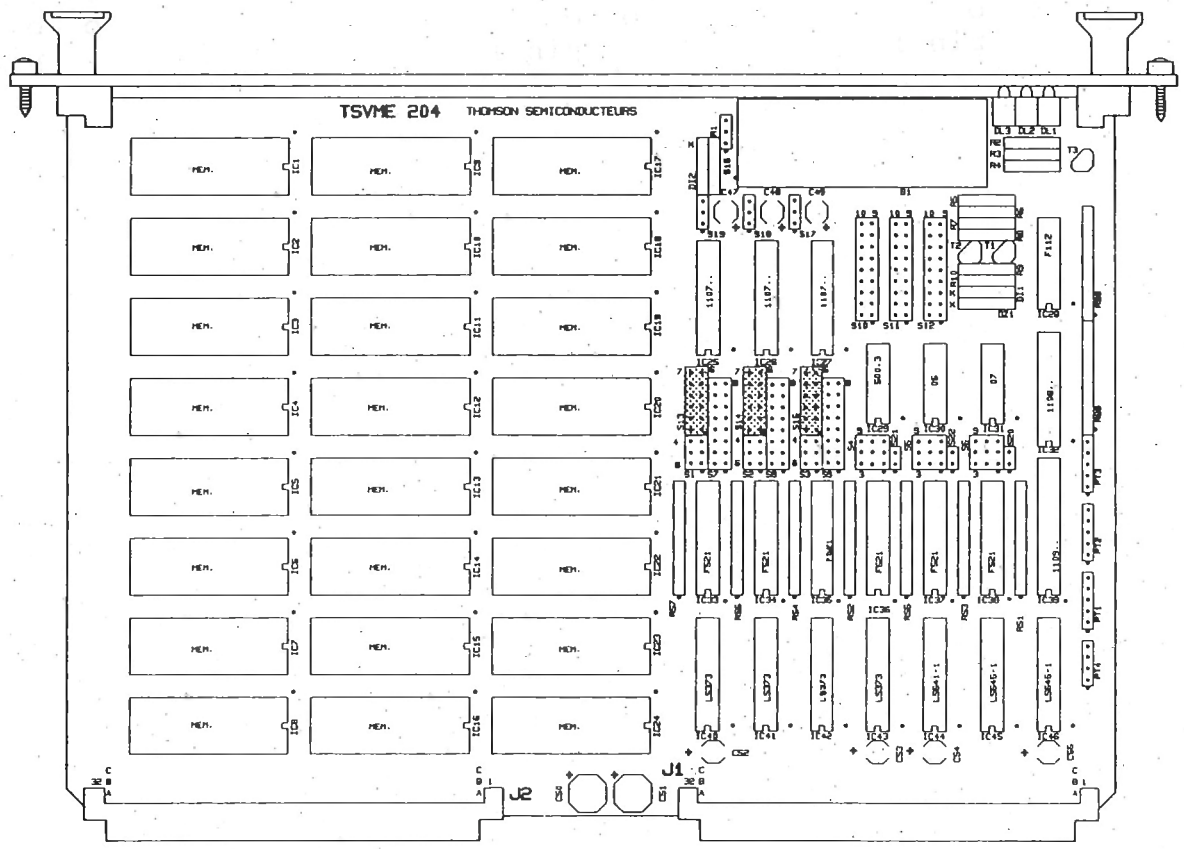
The jumper-selected access time corresponds to the time necessary for a data read on the unit with reference to its selection (pin 20).

The selectors S13, S14 and S15 enable access time to be selected for each block, blocks 3, 2,and 1 respectively.

Organization of the selectors S13, S14 or S15

```
o o  500ns
o o  350ns
o o  250ns
o o  200ns
o o  150ns
o o  100ns
  pin 1
```

The jumper should be positioned on the location higher or equal to the unit access time.
Location of the selectors S13, S14 and S15 on the board:



8.6 - SELECTION OF THE BACK-UP VOLTAGE SOURCE

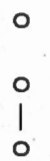
It is possible, by means of the local battery, to save a RAM STATIC memory block. The battery has a 40 mAh capacity, which allows a minimum back-up of 2 months for low consumption memories (up to 25 degrees C).

If a RAM memory which needs quite a high standby current is used, the on-board battery capacity is no longer sufficient and it will be necessary to provide an external back-up power supply source: by means of the VME bus +5V standby.

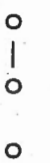
The jumper S16 allows the back-up voltage source to be selected : either by local battery
or by external battery (VME).

Jumper position on the selector S16:

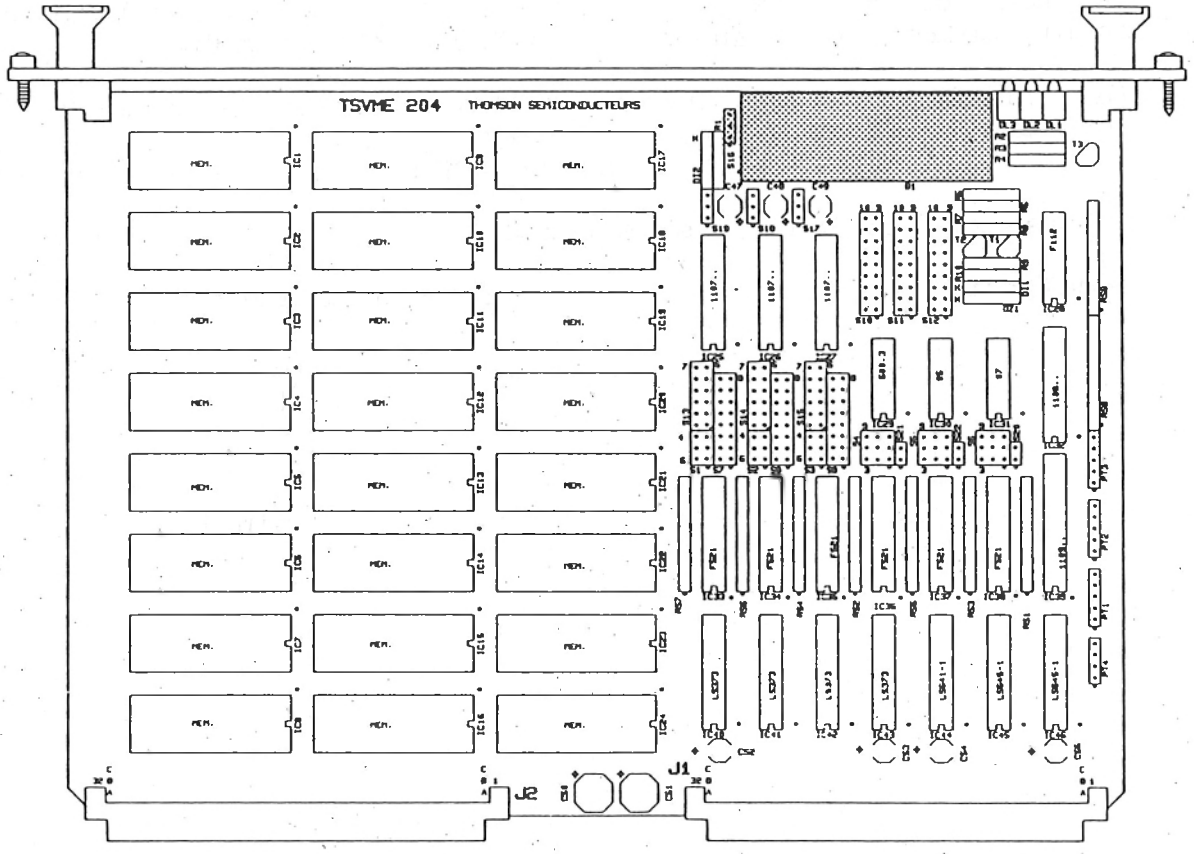
local battery



external battery



Location of the jumper S16 and the battery on the TSVME204 board



8.7 SELECTION OF THE BLOCK POWER SUPPLY SOURCE (BACK-UP OR NOT)

Jumpers S17-S18-S19:

The jumpers S17, S18 and S19 enable the power supply source to be selected for each block:

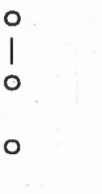
either the VME bus +5V
or the +5 back-up in case of mains failure

The local +5V back-up (see preceding chapter for the position of the jumper S16) can only be assigned to one block. (Problem of back-up duration).

Jumper position

For the 5V VME power supply

For the 5V back-up



8.8 WRITE ACCESS PROTECTION PER BLOCK

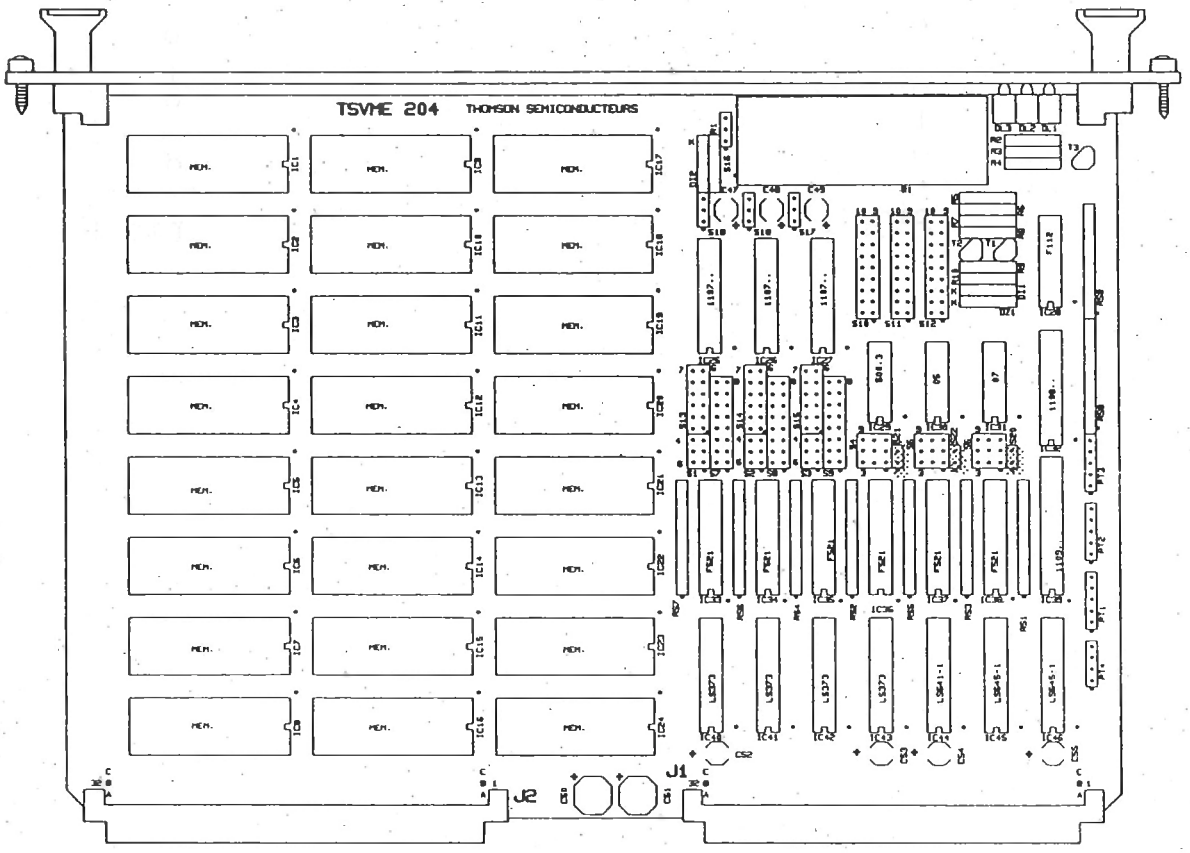
The jumpers S20, S21, S22 enable write access to be protected for each block.

Example of use : use of backed-up REPROM or RAM to which no further data modifications are to be made.

Jumper on : write and read access possible

Jumper absent : board non-selected for the protected block, on write.

Jumper location on the board



9 - BOARD START UP

9.1 - HARDWARE INSPECTION

Check that packing was not damaged during transportation.
Check that the board appears in perfect condition and in particular, that the circuits on sockets are correctly plugged in.

9.2 - POWER UP

Caution : the board may be damaged if plugged into a system which is already powered up.
The batteries equipping the TSVME204 boards are not charged.
In order to obtain a sufficient charge and subsequently a correct back-up, the board should be left powered up for a minimum of 20 hours before the back-up function works smoothly.

9.3 - START UP

- Configure the selectors with the help of the documentation
- Install the board in a VME chassis, board position does not affect system operation: all the "daisy chain" signals are chained on the board.
The VME chassis enables the board to be powered via the connectors P1 and P2.

ADDENDUM TO THE TSVME204 BOARD USER'S MANUAL

USE OF EEPROMS ON THE TSVME204 BOARD

Details on the installation of EEPROM devices on the TSVME204 board

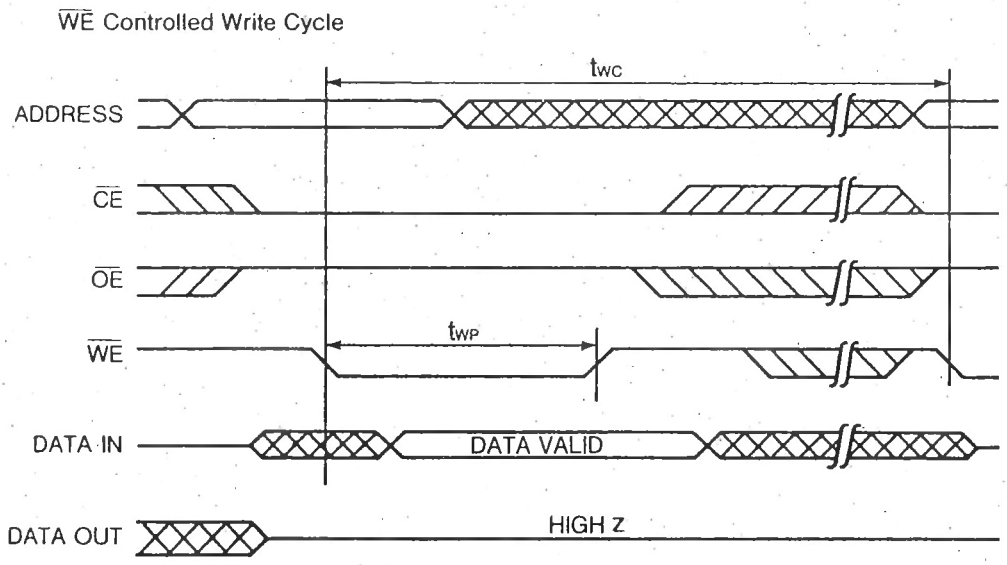
Only EEPROM devices with the following characteristics can be installed :

- All operations require a 5 V voltage only
- Storage of addresses and data by the devices in write mode
- On-board automatic sequencing of the device for write cycles
- JEDEC compatible pin configuration
- Internal data protection circuits to ensure data integrity after power failure or restart

* The EEPROM device will behave as a static RAM, as seen from the TSVME204 board.

  The user should be careful not to access the device for 10 ms after device write.

Sequencing of the various device signals during a write cycle :



* TWP is equal to the EEprom write access time (selected by S13, S14, S15.).

* TWC will software managed :

  Example : Timing loop following each EEPROM write access

NOTE : The BUSY*/READY signal available on some EEprom device makes is not used in order to ensure installation of a greater number of different devices. This signal will remain unconnected and will not be read in a register or another end of write cycle detection system.

Non exhaustive list of EEproms which can be used for the TSVME204 board :

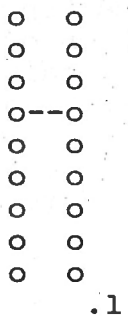
XICOR X2864A; -25; -35; -45
X2864AI; -25; -35; -45
X2864AM-25
X2864B
X2864M
X28C64
X28256

INTEL 2864; -2

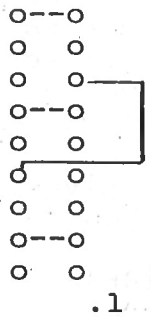
Connection configuration of S10, S11, S12 selectors for E2prom 8K x 8 and 32K x 8 devices

S10, S11, S12 selectors for devices :

E2prom 8K x 8

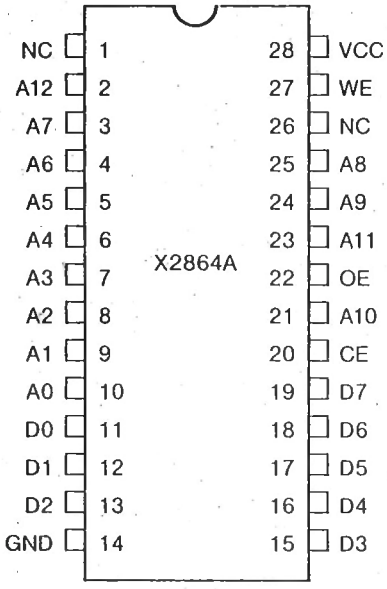


E2prom 32K x 8

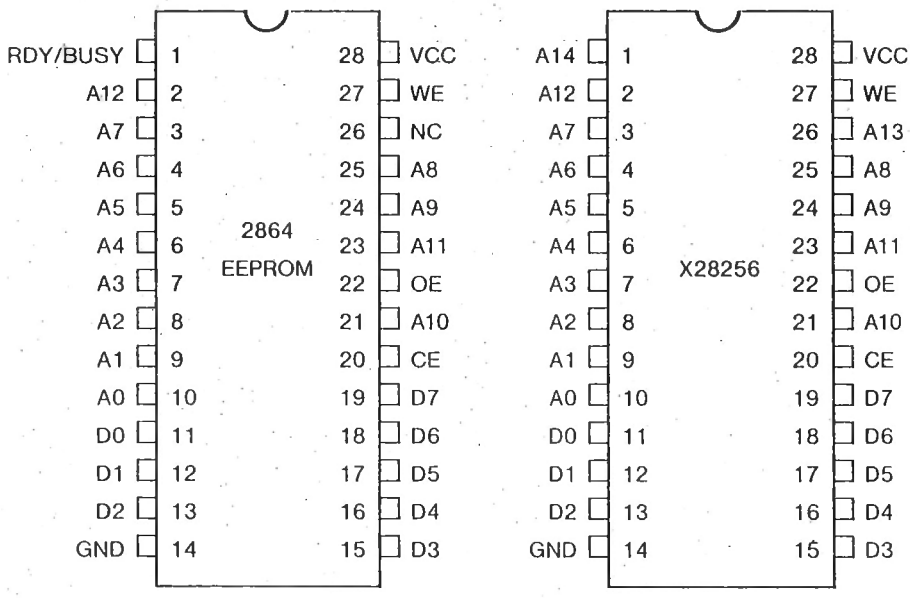


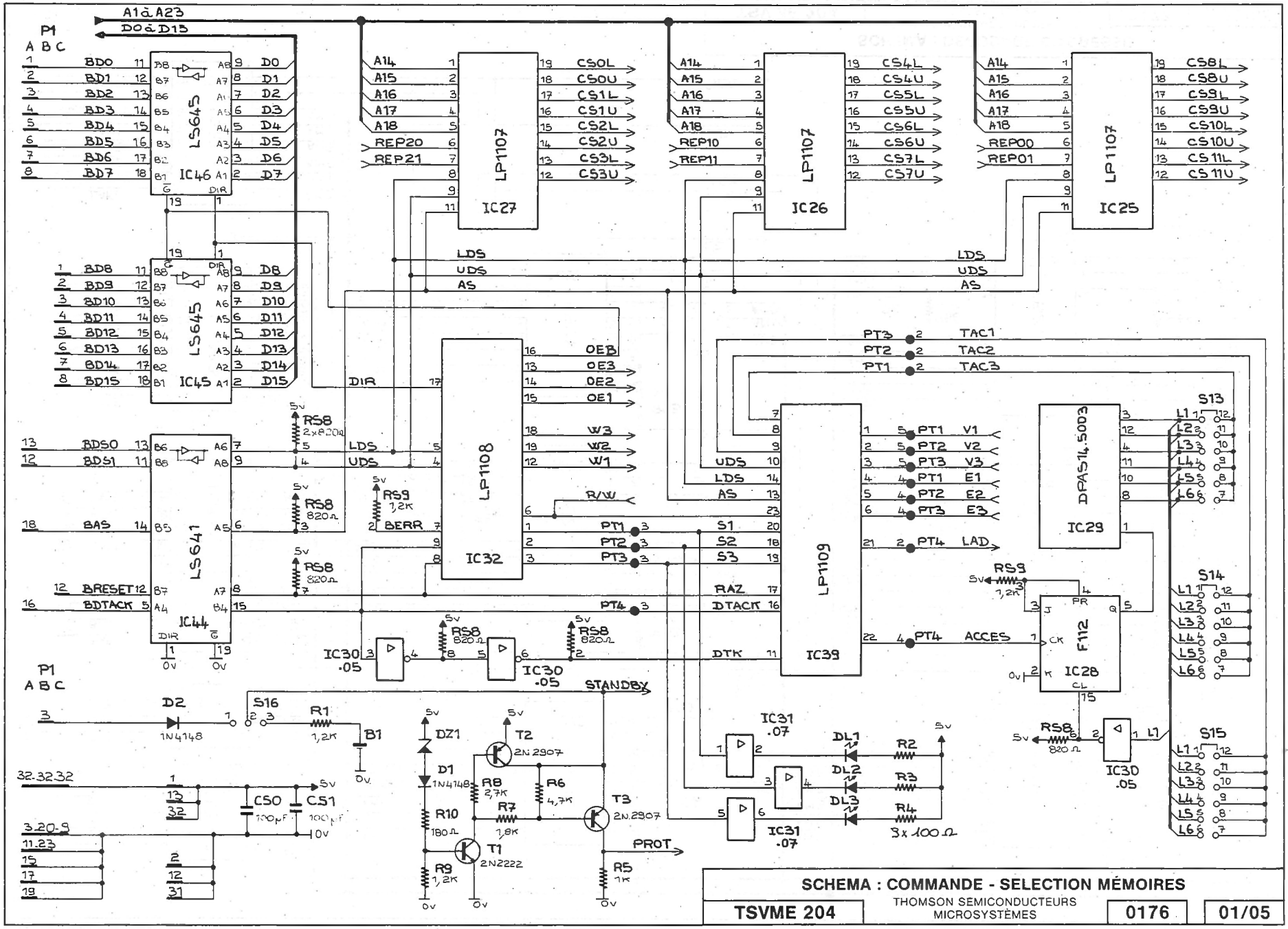
These configurations correspond to the following pin configurations :

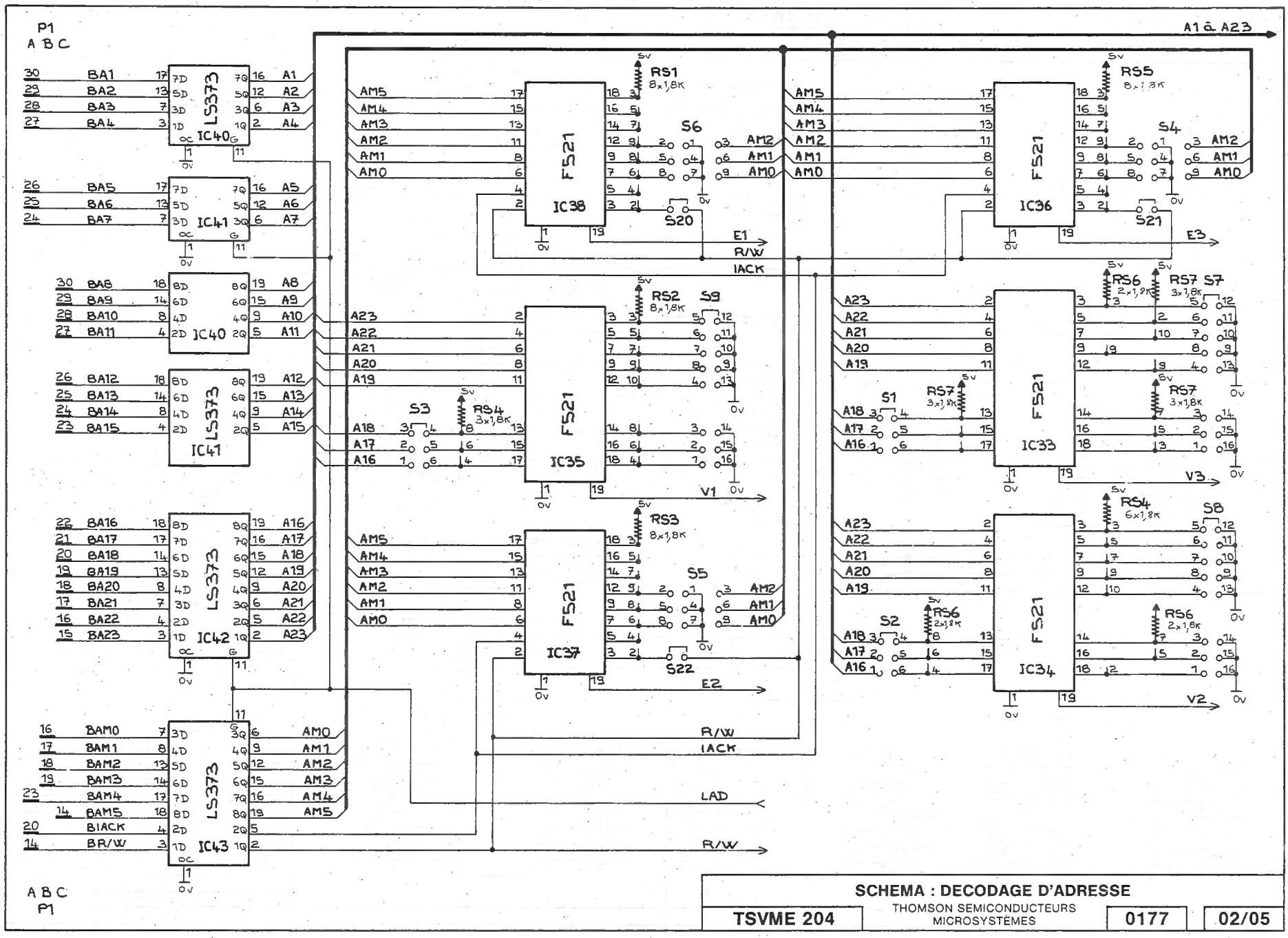
EEprom 8K x 8

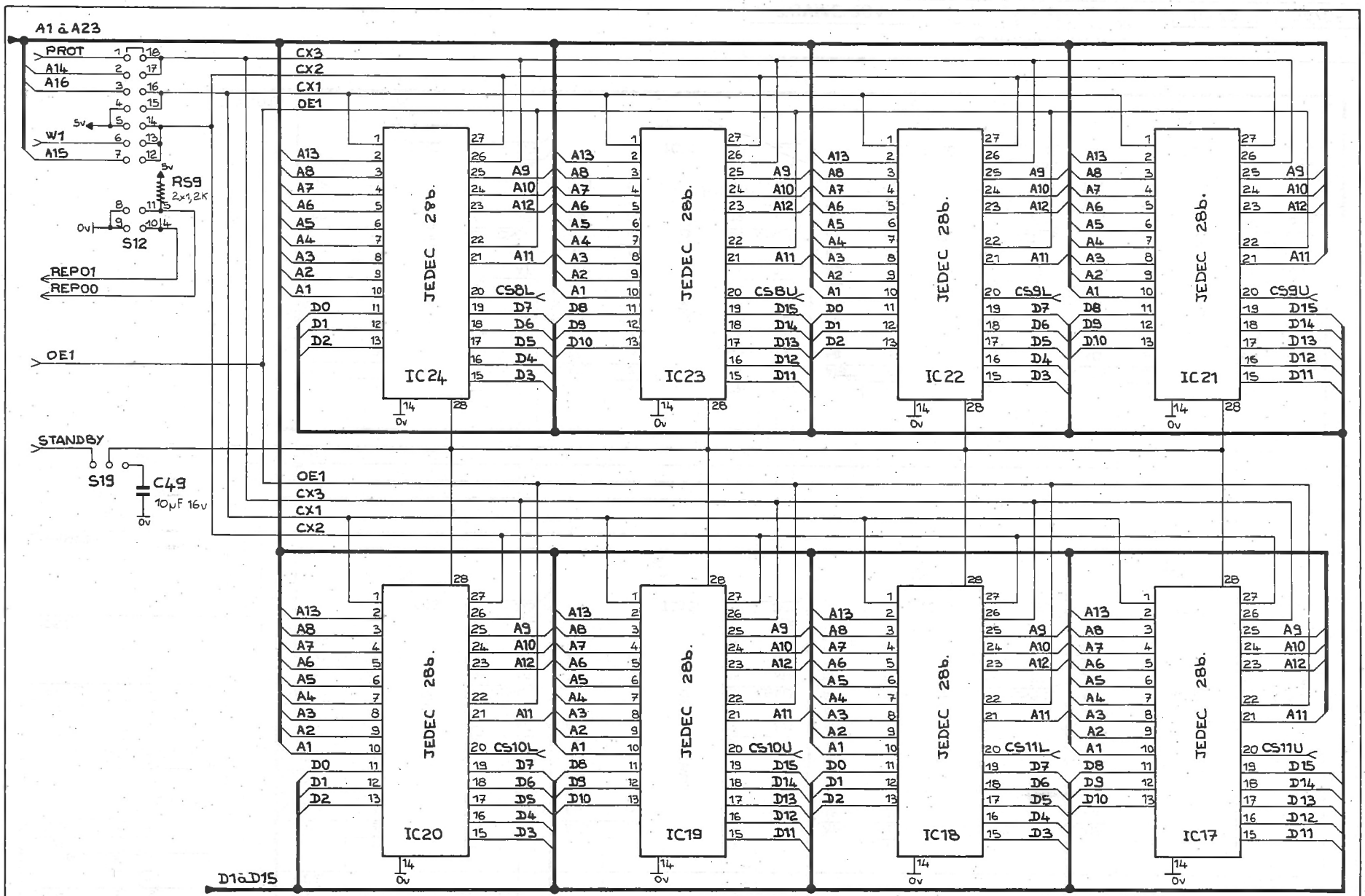


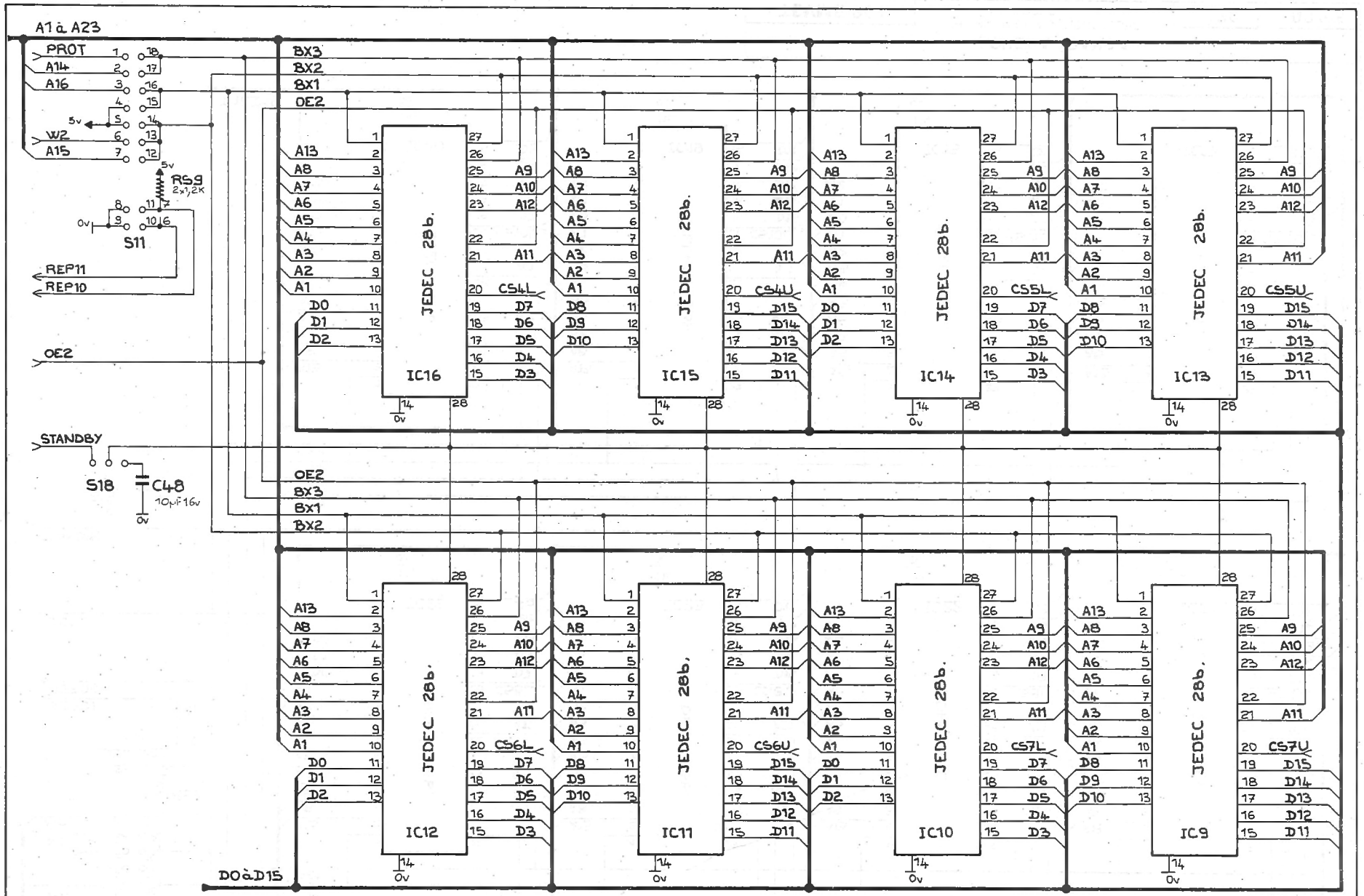
EEprom 32K x 8




A1 à A23
D0 à D15
P1
A B C
IC46 LS645
IC45 LS645
IC44 LS641
IC27 LP1107
IC26 LP1107
IC25 LP1107
IC32 LP1108
IC39 LP1109
IC29 DPAS14.5003
IC28 F112
IC30 .05
IC31 .07
IC30D .05
LDS
UDS
AS
DIR
R/W
BERR
BAS
BRESET
BDTACK
RAZ
DTACK
DTK
STANDBY
PROT
ACCES
PT1
PT2
PT3
PT4
TAC1
TAC2
TAC3
S13
S14
S15
DL1
DL2
DL3
3x 100 Ω
SCHEMA : COMMANDE - SELECTION MÉMOIRES
TSVME 204
THOMSON SEMICONDUCTEURS
MICROSYSTÈMES
0176
01/05


P1
A B C
A1 à A23
LS373
IC40
IC41
IC42
IC43
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
BA11
BA12
BA13
BA14
BA15
BA16
BA17
BA18
BA19
BA20
BA21
BA22
BA23
BAM0
BAM1
BAM2
BAM3
BAM4
BAM5
BIACK
BR/W
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
AM0
AM1
AM2
AM3
AM4
AM5
FS21
IC38
IC36
IC35
IC33
IC37
IC34
RS1
RS2
RS3
RS4
RS5
RS6
RS7
S1
S2
S3
S4
S5
S6
S7
S8
S9
S20
S21
S22
E1
E2
E3
R/W
IACK
LAD
V1
V2
V3
5V
0V
SCHEMA : DECODAGE D'ADRESSE
TSVME 204
THOMSON SEMICONDUCTEURS
MICROSYSTÈMES
0177
02/05


A1 à A23
PROT
A14
A16
W1
A15
5v
RS9
2x1,2K
S12
0v
REPO1
REPO0
OE1
STANDBY
S19
C49
10µF 16v
CX3
CX2
CX1
OE1
JEDEC 28b.
IC24
IC23
IC22
IC21
IC20
IC19
IC18
IC17
CS8L
CS8U
CS9L
CS9U
CS10L
CS10U
CS11L
CS11U
D1à D15
SCHEMA : BANC 1
THOMSON SEMICONDUCTEURS
MICROSYSTÈMES
TSVME 204
0178
03/05



SCHEMA : BANC 2

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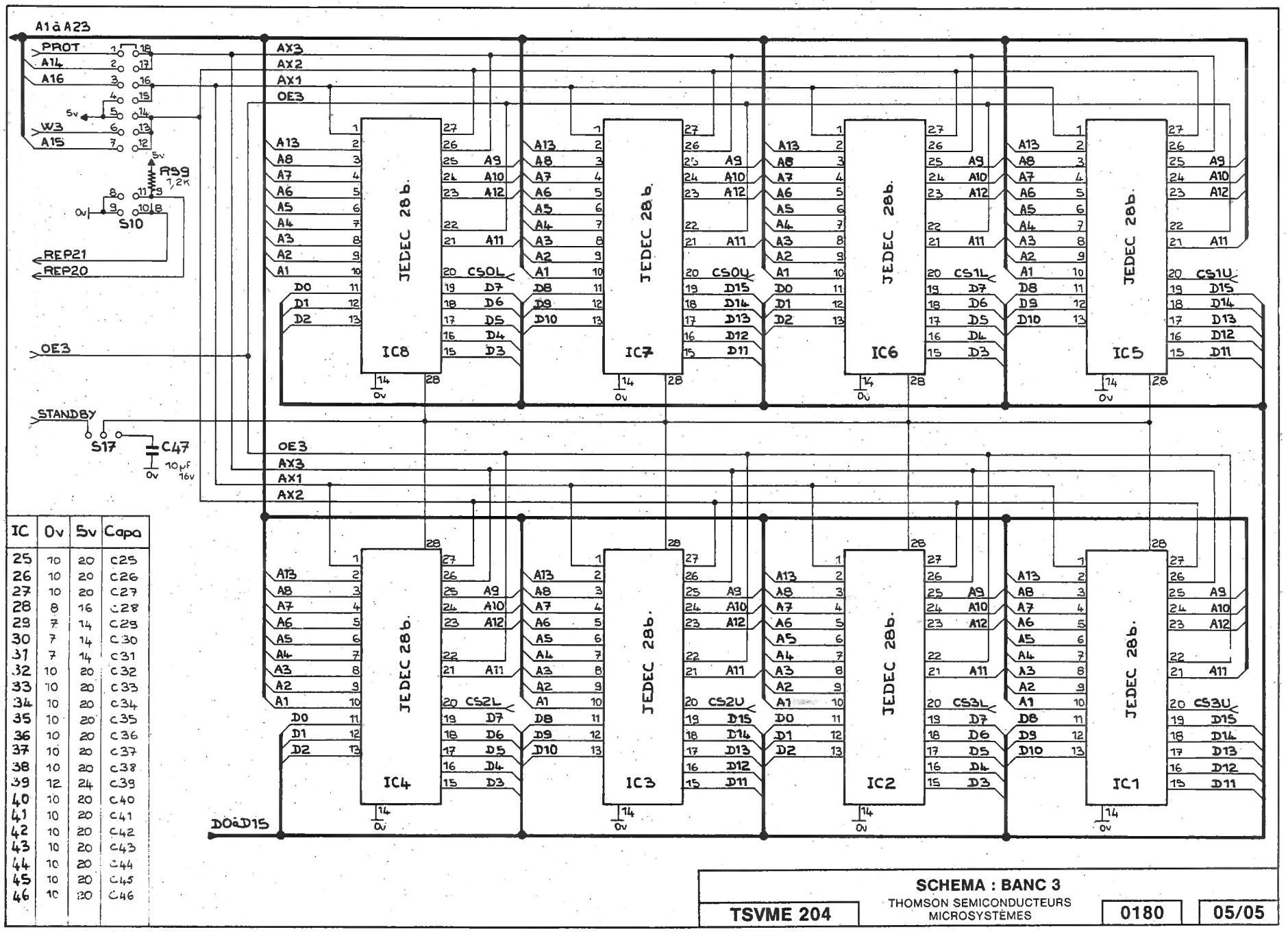

IC	0v	5v	Capa
25	10	20	C25
26	10	20	C26
27	10	20	C27
28	8	16	C28
29	7	14	C29
30	7	14	C30
31	7	14	C31
32	10	20	C32
33	10	20	C33
34	10	20	C34
35	10	20	C35
36	10	20	C36
37	10	20	C37
38	10	20	C38
39	12	24	C39
40	10	20	C40
41	10	20	C41
42	10	20	C42
43	10	20	C43
44	10	20	C44
45	10	20	C45
46	10	20	C46

SCHEMA : BANC 3

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