27513
PAGE-ADDRESSED 512K (4 x 16K x 8) UV ERASABLE PROM

- **Paged Organization**
  - **— Reduced Physical Address Requirement**
  - **— No Bank Switching Logic Needed**
- **Software Carrier Capacity**
- **Automatic Page Clear**
  - **— Resets to Page 0 on Power Up and On Demand with $\overline{RST}$ Signal(1)**
- **TTL and CMOS Compatible**
- **170 ns Access Time**
- **Two Line Control**
- **Low Power**
  - **— 125 mA max. Active**
  - **— 40 mA max. Standby**
- **Compatible with Industry Standard EPROM Pinouts**
  - **— Direct 27128A Compatibility**
  - **— 28-Pin Cerdip**

The Intel 27513 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory. It is organized as 4 pages of 16K 8-bit words. The 27513's paged organization brings 64 K-byte storage capacity to existing 128K EPROM-based designs and to popular 8-bit microprocessor or microcontroller systems that have 64 K-byte total addressing capability. The 27513 provides an ideal means of quadrupling current 16 K-byte code space.

The 27513's large storage capability of 64 K-bytes and 170 ns access time enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27513 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The 27513 has an automatic page clear circuit for ease of use of the page-addressed organization. The page-select latch is automatically cleared to the lowest order page upon system power up.

Two-line control and industry standard 28-pin packaging are features common to all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27513 is manufactured using Intel's Compacted HMOS* II technology.

NOTE:
1. $\overline{RST}$ feature only available on devices with 6-digit suffix.

September 1989
Order Number: 231113-007

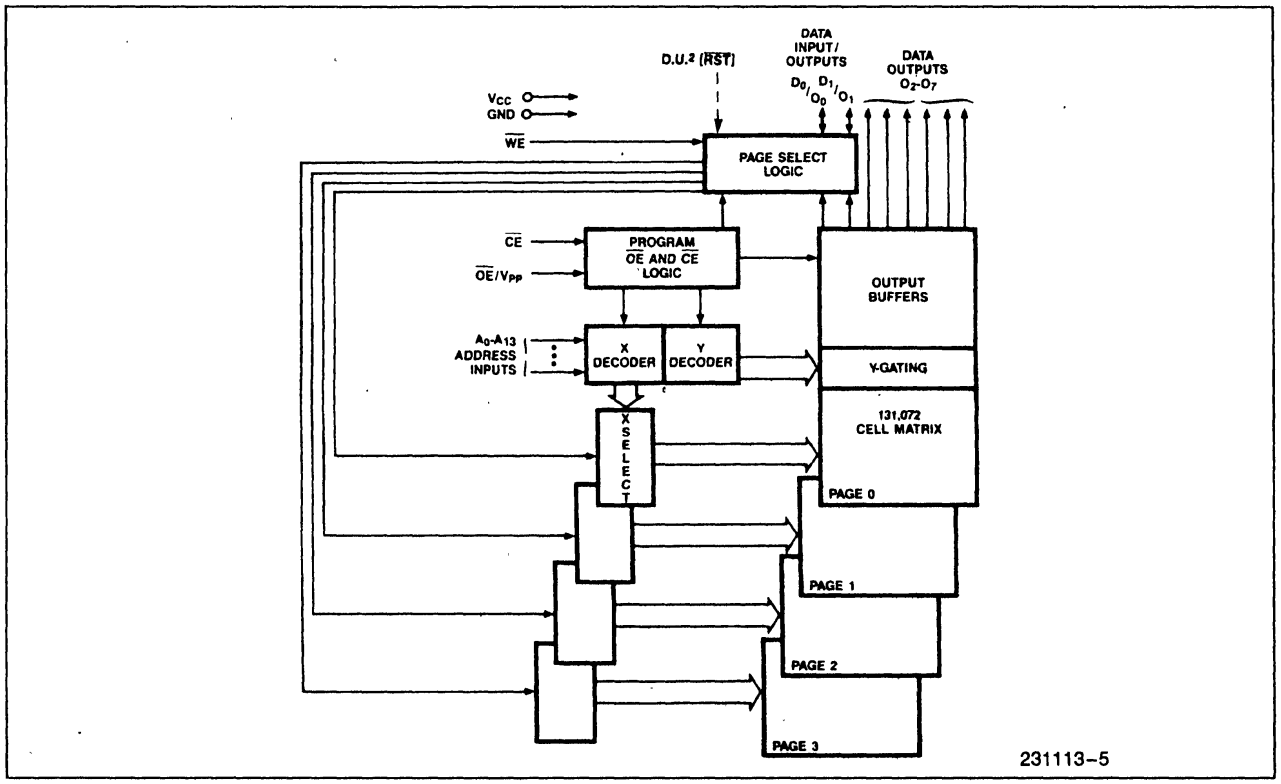
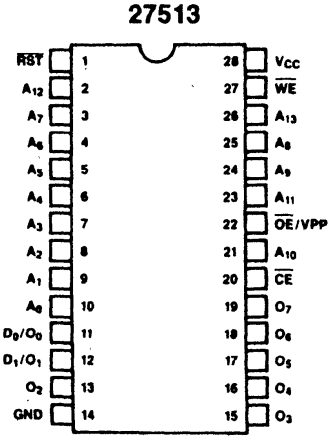


Figure 1. Block Diagram

2716	2732A	2764A 27C64 87C64	27128A 27C128	27256 27C256	27512 27C512
		V_{PP}	V_{PP}	V_{PP}	A_{15}
		A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND	GND



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27512 27C512	27256 27C256	27128A 27C128	2764A 27C64 87C64	2732A	2716
V_{CC}	V_{CC}	V_{CC}	V_{CC}		
A_{14}	A_{14}	$\overline{PGM}$	$\overline{PGM}$		
A_{13}	A_{13}	A_{13}	N.C.	V_{CC}	V_{CC}
A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	V_{PP}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3

Figure 2. Pin Configuration

NOTES:
1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27513 pins.

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
$\overline{WE}$	Page-Select Write Enable
O_2–O_7	Outputs
D_0/O_0,D_1/O_1	Input/Outputs
$\overline{RST}$	Page Reset(1)

NOTE:
1. $\overline{RST}$ feature only available on devices with 6-digit suffix.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.15 electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27513 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-200V10	Q, L, T

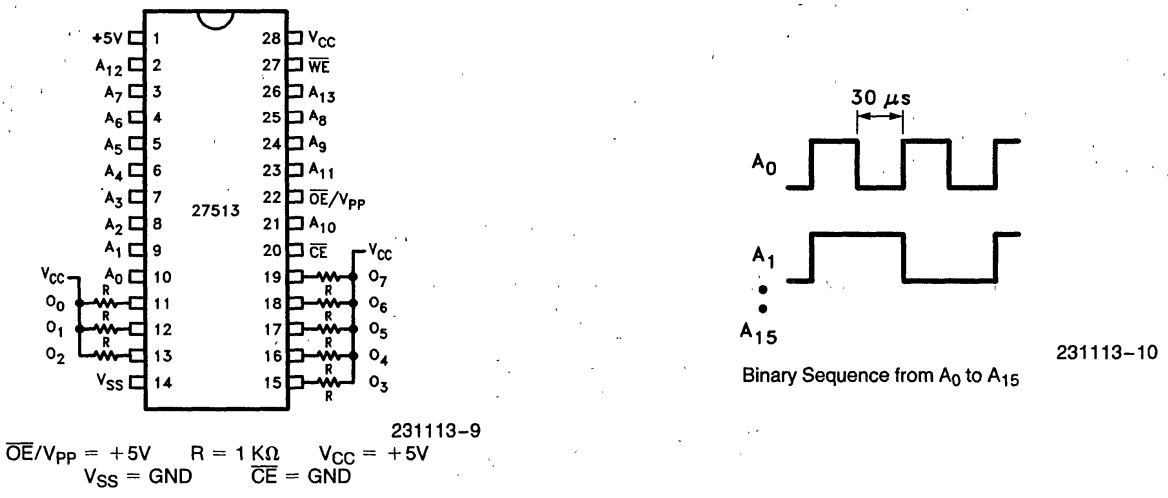
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27513 LD27513		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE}/V_{PP} = V_{IL}$
I_{CC_1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground† ..... −0.6V to +6.5V
Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V
$\overline{OE}/V_{PP}$ Supply Voltage with
Respect to Ground ..... −0.6V to +14.0V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7.0V

† includes Don't Connect (pin 1)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ AND PAGE-SELECT WRITE OPERATIONS

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{SB}(4)	V_{CC} Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(4)	V_{CC} Current Active		90	125	mA	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage		3.5	4.0	V	

READ OPERATION

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions(5)		V_{CC} ±5%	27513-170V05		27513-2 27513-200V05		27513		Units	Test Conditions
		V_{CC} ±10%	27513-170V10		27513-20 27513-200V10		27513-25			
Symbol	Parameter		Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay			170		200		250	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			170		200		250	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay			60		75		100	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}/V_{PP}$ High to Output Float		0	50	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First		0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

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PAGE-SELECT WRITE AND PAGE-RESET OPERATION

A.C. CHARACTERISTICS

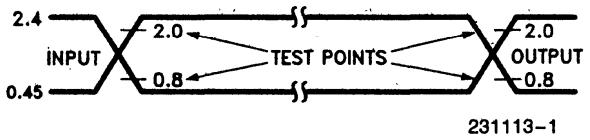
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	180		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time	55		ns	
t_{RST}	Reset Low Time	250		ns	
t_{RAV}	Reset to Address Valid	250		ns	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP; N = PLCC.
6. $\overline{RST}$ function is available only on parts with 6-digit suffix.

CAPACITANCE(2) T_A = +25°C, f = 1 MHz

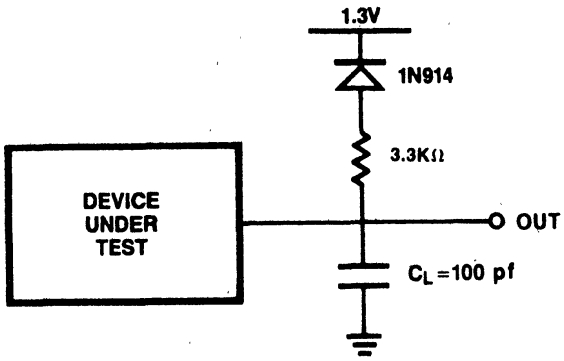
Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
$C_{\overline{OE}/V_{PP}}$	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	V_{IN} = 0V

A.C. TESTING INPUT/OUTPUT WAVEFORM



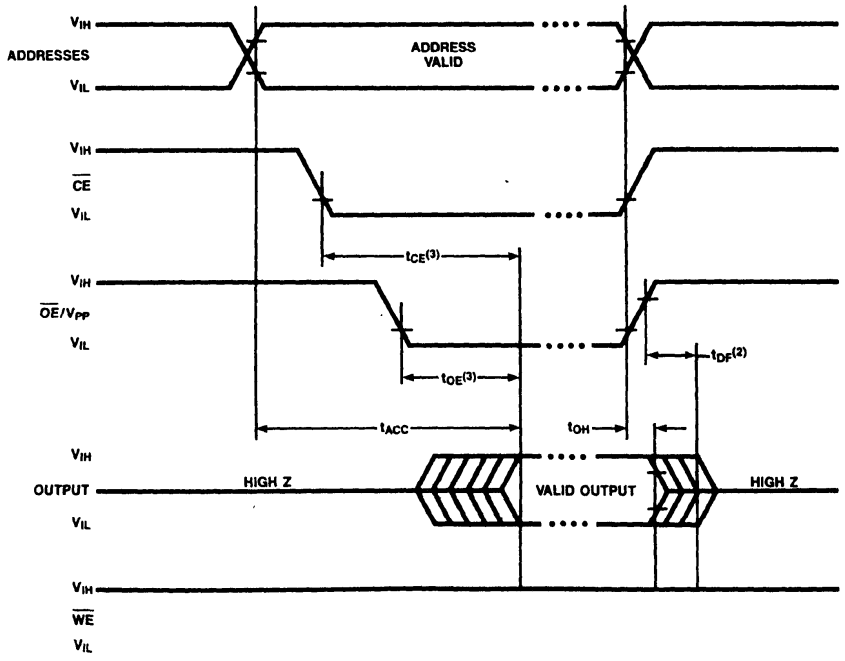
AC Testing inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS FOR READ OPERATION



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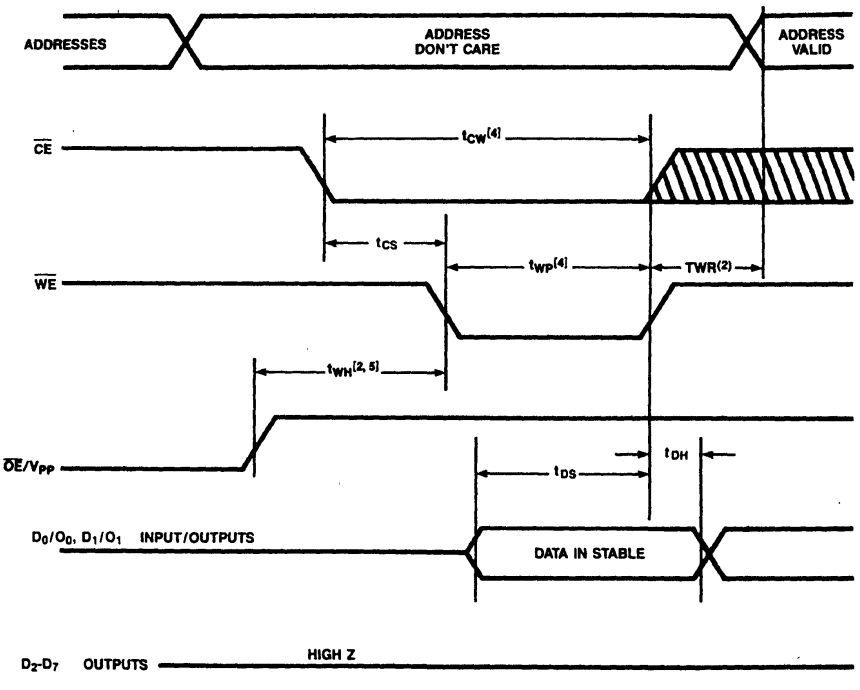
A.C. WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



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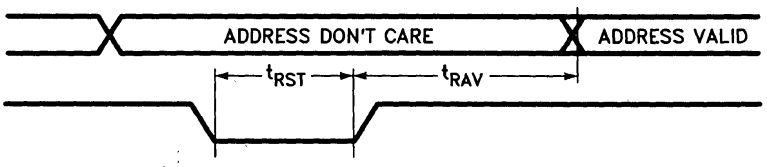
A.C. WAVEFORMS FOR PAGE-RESET OPERATIONS



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NOTES:
1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}/V_{PP}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27513 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for int$_e$ligent Identifier mode.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	$\overline{RST}$	A_9	A_0	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X(1)	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	V_{IH}	X	X	V_{CC}	High Z	High Z
Programming	V_{IL}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	(Note 3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	V_{CC}(5)	High Z	Page(2) D_{IN}
Page-Reset	X	X	X	V_{IL}	X	X	V_{CC}(5)	High Z	X
int$_e$ligent(4) —Manufacturer Identifier	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IL}	5.0V	89H	89H
—Device	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IH}	5.0V	0FH(6)	0FH(6)

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 2 for V_{CC} and V_{PP} voltages.
4. A_1-A_8, $A_{10}-A_{13}$, $= V_{IL}$.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. 27513s before 2H/86 have a device identifier of 0DH. 27513s after 2H/86 will have a device identifier of 0FH.
7. $V_H = 12.0V \pm 0.5\%$.

Read Mode

The 27513 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

The 27513 has a standby mode which reduces the maximum active current from 125 mA to 40 mA. The 27513 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27513 is addressed by first selecting one of four 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0 and D_1/O_1. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output (Pin) Page Selection	D_1/O_1 (12)	D_0/O_0 (11)
Select Page 0	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}
Select Page 2	V_{IH}	V_{IL}
Select Page 3	V_{IH}	V_{IH}

Page Reset

The 27513 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case −10% V_{CC} supply condition) against spurious page latch clearing.

27513 parts with 6-digit suffixes also have a page reset pin: $\overline{RST}$. This pin should be tied to an active low system reset signal. These 27513s will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27513s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by

properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the 27513.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ input is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27513s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27513s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27513s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at its programming voltage will program the selected 27513.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

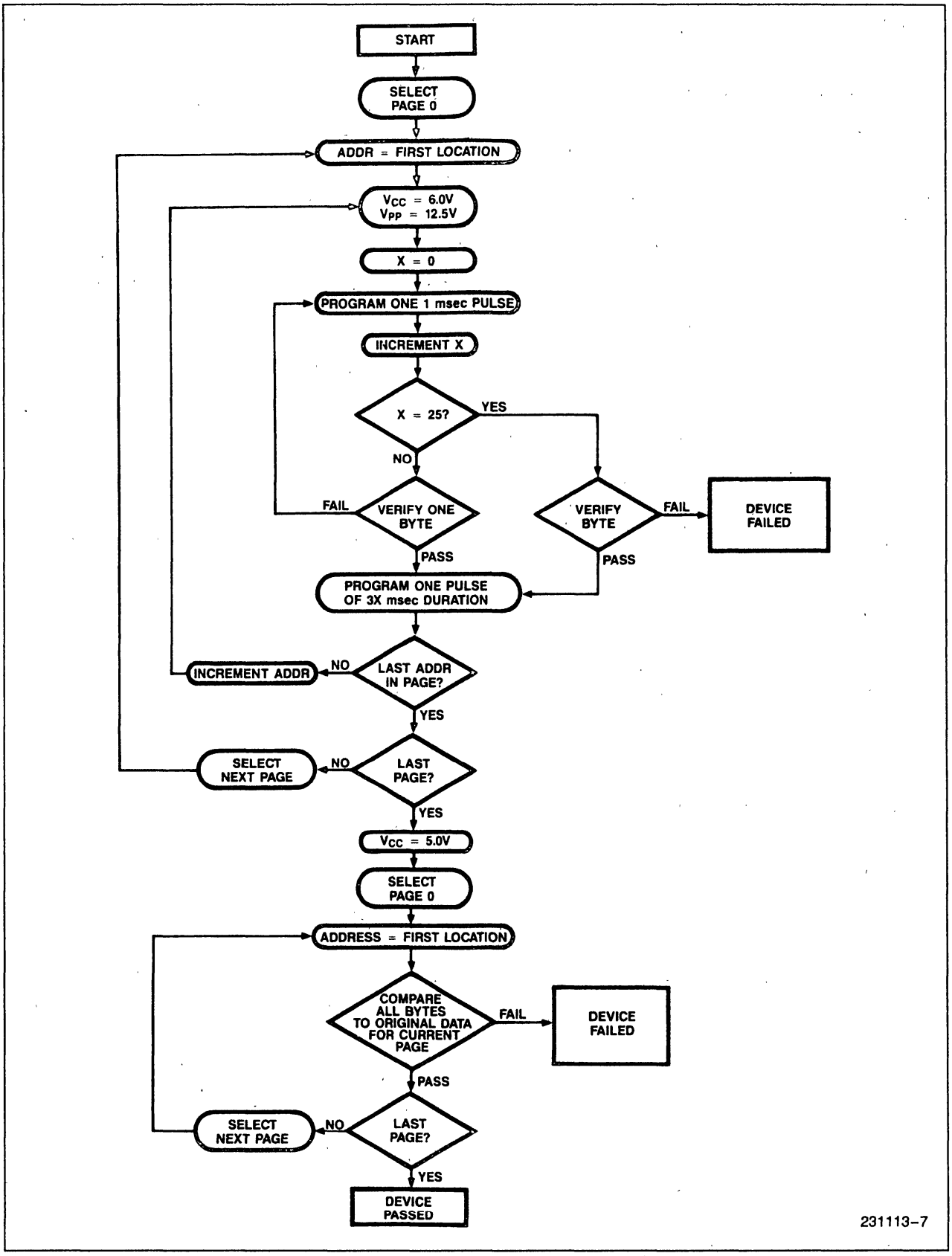


Figure 5. 27513 Int$_e$ligent Programming™ Flowchart

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

inteligent Programming™ ALGORITHM

The inteligent Programming Algorithm programs Intel EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of six minutes. Actual Programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27513 inteligent Programming Algorithm is shown in Figure 3. The only difference between the 27513 and other EPROM inteligent Programming is that the 27513 is programmed one 16 K-byte page at a time.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400 μA
I_{CC2}(2)	V_{CC} Supply Current (Program and Verify)		125	mA	
I_{PP2}(2)	V_{PP} Supply Current (Program)		40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 inteligent Identifier Voltage	11.5	12.5	V	
V_{PP}	inteligent Programming Algorithm	12.0	13.0	V	
V_{CC}	inteligent Programming Algorithm	5.75	6.25	V	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0–O_7 unloaded.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied. ***The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V.*** When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

A.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 3)
t_{VCS}	V_{CC} Setup Time	2			µs	(Note 1)
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			µs	
t_{DV}	Data Valid from $\overline{CE}$			1	µs	
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			µs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

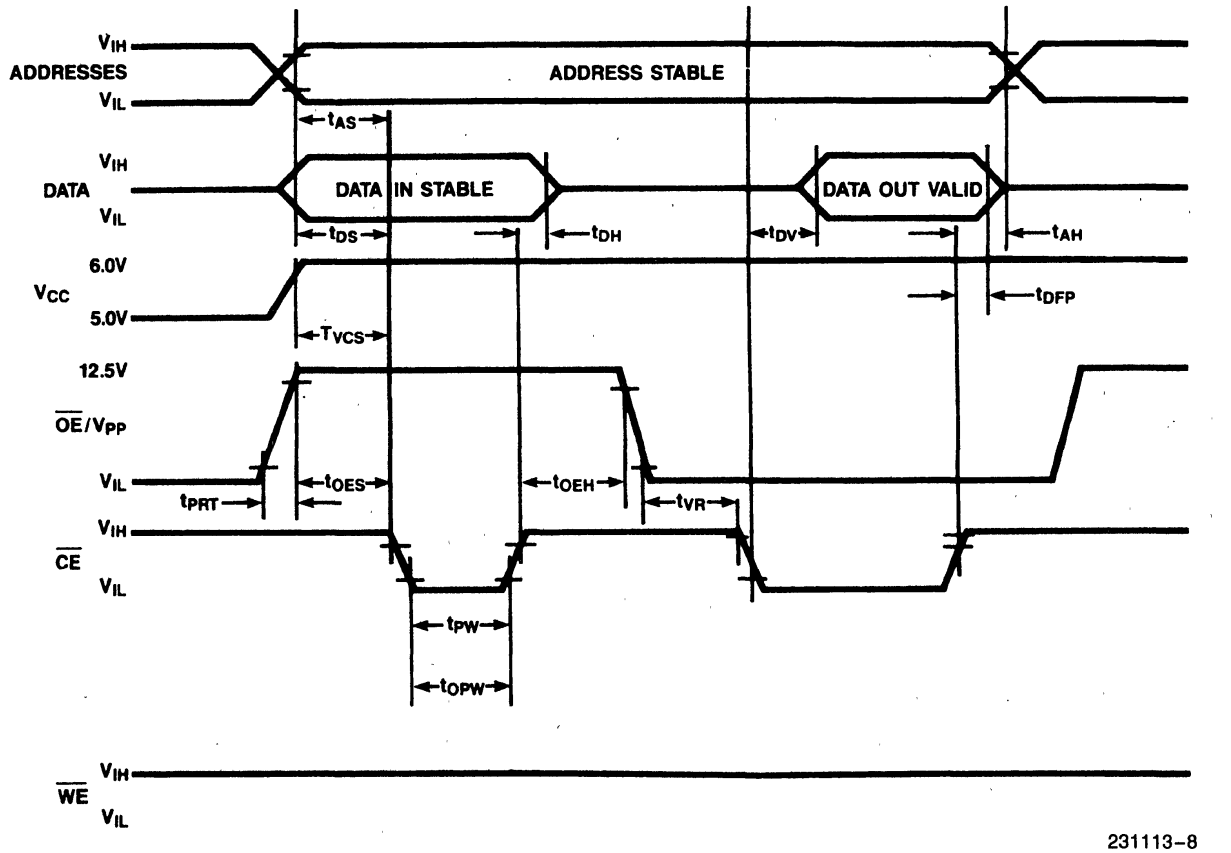
*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse (int$_e$ligent Programming Algorithm only) may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

5

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 K-byte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

REVISION HISTORY

Number	Description
07	Revised Express Options Revised Pin Configuration D.C. Characteristics-I_{LI} Test Conditions-V_{IN} = **0V to V_{CC}** D.C. Characteristics-I_{LO} Test Conditions-V_{OUT} = **0V to V_{CC}**